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Introduction to Switching Theo
& Logical Design

Introduction to Switching Theory & Logical Design

SECOND EDITION

Frederick J. Hill
Gerald R. Peterson

WILEY INTERNATIONAL EDITION

introduction to
SWITCHING THEORY AND LOGICAL DESIGN

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SECOND EDITION

Fredrick J. Hill
Professor of Electrical Engineering
University of Arizona

Gerald R. Peterson
Professor of Electrical Engineering
University of Arizona

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Preface

In the field of digital computers, there is an area somewhere between circuit design and system formulation which is usually identified as switching theory. Although this topic must be mastered by the digital computer engineer, it does not answer all the questions concerning layout of an efficient digital computing system. The remaining questions, which are less susceptible to formalization, may be grouped under the heading "Digital System Theory."

Our approach is to follow the basic framework of switching theory. We hope, however, to motivate the student by presenting examples of the many problems which appear repeatedly in the design of digital systems. It is not our intent to provide the student with a detailed knowledge of such specialized system topics as computer arithmetic. Instead, we attempt to provide the framework through which the student might develop a sound design philosophy applicable to any digital design problem. Thus, we do not feel that the use of the term "logical design" in the title is unjustified.

The usefulness of switching theory is not restricted to engineers actively engaged in computer design. In fact, it is our contention that almost every design engineer in the field of electronics will have some opportunity to draw on this subject. Applications occur whenever information in communication, control, or instrumentation systems, for example, is handled in other than analog form.

The above three paragraphs, which began the preface of the First Edition of this book, seem to us to be even more accurate today than they were six years ago. In these years, digital techniques have become virtually standard in many areas once considered the exclusive preserve of analog techniques. This "digitalization" of electrical engineering has become so pervasive that it is a rare electrical engineer who will not have some contact with digital design problems.

We undertook preparation of this second edition in order to strengthen some of the pedagogical weak spots of the first edition as well as to include new material made necessary by recent developments, particularly in the area of integrated circuits. As an example of the latter, we have rewritten

Chapter 5 and added Chapter 16 to reflect the general acceptance of integrated circuits and LSI throughout industry. We have completely reworked Chapters 9–13 and have added Chapters 14 and 15 on sequential circuits. The emphasis of these chapters has shifted toward creative design and away from formal minimization. This will be most apparent in Chapter 15, which describes a digital hardware design language. We found the original treatment in Chapters 2, 3, 4, 6, and 7 to be quite satisfactory and have made few changes except in the problem sets. Considerable effort has been devoted to updating and improving the problems throughout the book.

Chapters 1 and 2 were written with the goal of providing student motivation. We have endeavored to sustain this motivation throughout the book by treating with special care points which might otherwise become sources of confusion. It is our belief that, if questions concerning justifications behind manipulative procedures go unanswered, the student will be discouraged. Our intention to avoid such pitfalls is exemplified in Chapter 4 by a reliance on Huntington's original postulates and careful distinction between the algebra of the Karnaugh map and the two-valued algebra of truth values. (This is essentially the same as the distinction between Boolean forms and switching functions, which is made with great care in some more advanced texts.) Our treatment of Boolean algebra is formal to be sure, but we have found that it represents no conceptual difficulties to the student.

The introductory chapter should occupy no more than one day of class time, or it could be left as a reading assignment if class time is critical. The binary number system is taken up in Chapter 2 to provide a background for the binary notation of Boolean functions and maps in Chapters 4 and 6. The subject is allotted a separate chapter which is placed prior to the introduction of Boolean algebra to minimize the chance of confusing the two concepts. The additional material on binary arithmetic is essential only for examples and might be omitted, or referred back to, if desired.

Chapters 3 and 4 provide the basic logical and algebraic basis for switching theory and certainly have not diminished in importance in any way. We believe the benefits to the students will be great if the topics of these chapters are covered in order with no omissions. Chapter 5, on components, has been totally rewritten to reflect the almost total replacement of discrete logic circuits by integrated circuits. The coverage of this chapter may be adjusted to suit the purposes of the instructor.

Chapters 6 and 7 remain unchanged in the second edition except for new problem sets. Rapid developments in components, particularly integrated circuits, have greatly changed the relative importance of various cost factors in digital design, but the basic correlation between simple algebraic forms and economical designs remains undisturbed. And we believe the Karnaugh map and Quine-McCluskey minimization remain unchallenged as the most natural, powerful, and widely applicable tools for simplifying switching functions. These two chapters should be covered in detail.

From Chapter 8 on, the book has been almost totally rewritten. Chapter 8 has been expanded to include additional topics related to integrated circuit realization of certain specialized combinational circuits. Included is a section on the use of programmable read-only memories as generalized logic elements. Chapter 9 has been expanded to include a fairly extensive coverage of flip-flops and comparison between the various types of sequential circuits and their timing characteristics.

Chapter 10, on clocked sequential circuits includes an improved treatment of the problem of setting up the initial state table and a better discussion of state assignment. State assignment is certainly the most difficult aspect of sequential circuit design. The literature includes many papers dealing with various sophisticated and complex state assignment techniques which rarely produce results which can justify the time and effort required to learn and apply them. We present a more intuitive approach which relies heavily on the designer's natural *a priori* insight into the structure ultimately required and which will provide satisfactory assignments for a reasonable expenditure of effort.

The pulse mode circuits material has been moved from Chapter 12 in the First Edition to Chapter 11 and changed only slightly. This provides a smoother transition into incompletely specified circuit examples. The treatment of incompletely specified circuits, now in Chapter 12, has been simplified to avoid undue emphasis on state table minimization. The Grasselli-Luccio minimization procedure is now covered in Appendix A.

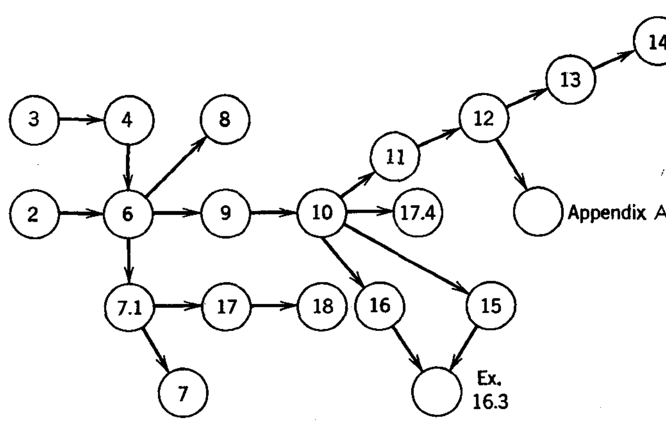
Chapter 13 is totally rewritten, to provide adequate coverage of the general class of "nonpulsed" circuits, which we have christened "level mode circuits" and of which fundamental mode is only a special case. In particular, we have expanded the treatment of race-free assignments and have covered circuits in which two or more inputs may change simultaneously.

Chapter 14 is entirely new and presents a method of hazard-free level mode design which has apparently been used by integrated circuit designers but which, to the best of our knowledge, has never before been treated in a textbook. Chapter 16, also new, introduces some of the special problems of logic design involving medium-scale and large-scale integrated circuits.

As noted earlier, it is generally recognized that the formal techniques of switching theory, or logic design, do not extend readily to the design of larger systems. In the area of system design, register transfer languages are gaining wide acceptance. Our companion volume, *Digital Systems: Hardware Organization and Design* (Wiley, 1973) provides a thorough treatment of the application of a register transfer language to the design of large-scale digital systems. Chapter 15 of this book attempts to "bridge the gap" through application of a simplified register transfer language to the design of circuits which are too large to be efficiently attacked by the logic design methods presented earlier but are not large enough to be considered full-scale digital systems in the usual sense. The reader who has used both texts will notice a difference in the primary hardware implementation of the control unit in the two books. In this book, we rely on the reader's familiarity with standard clock mode sequential circuits, while in the other book we introduced a special element called the control delay. In that book, we were primarily concerned with describing large digital hardware systems to students who may or may not have been expert in sequential circuits. The language used in Chapter 15 to describe hardware will be a subset of and completely consistent with the AHPL of the other book. Once a reader has become familiar with both developments, he will have no difficulty switching between the two hardware interpretations.

Chapters 17 and 18 (Chapters 14 and 15 of the First Edition) are little changed except for the addition of material on iterative circuits to Chapter 17. This is a topic of considerable importance in the design of integrated circuits, where the use of repetitive structures may lead to significant economies. Chapter 16 of the First Edition, on linear circuits and codes, was written because, at that time, there was no satisfactory undergraduate text on this subject. In the interim, excellent texts have appeared, so this chapter has become superfluous.

The diagram illustrates the prerequisite relationships between the various chapters, as an aid to instructors in planning courses based on this book. It can readily be seen from the chart that Chapters 2, 3, 4, 6, 9, and 10 would necessarily be included in most any course structure. Beyond this, the



instructor has considerable freedom in structuring the course. Of the remaining restrictions, the most critical is that the level mode material of Chapters 13 and 14 has as a prerequisite the incompletely specified state table minimization of Chapter 12, which in turn requires Chapter 11. One perfectly satisfactory approach is to take up the chapters in numerical order. Another alternative which may be attractive to instructors wishing to expose their students to some system design problems would be to take up Chapters 15 and 16 after Chapter 10. These two chapters contain a number of system design examples of varying degrees of complexity. Where students already have a background in combinational logic, a course can be begun with any of Chapters 7, 8 or 9. There is more than enough material of practical value to constitute a one semester course beginning with Chapter 9.

Finally, we might note that for logic symbols we have retained the uniform shape symbols of standard IEEE No. 91-A.S.A. Y 32.14-1962. After this book went into production, a new standard IEEE No. 91-ANSI Y 32.14-1973 appeared. It is the first standard to be adopted by all concerned agencies, both civilian and military, in the United States, and is in substantial agreement with international standards. As such it represents a long overdue step toward standardization, which we heartily applaud. Unfortunately, it appeared too late to be included in this book, except for some special cases. The differences between this new standard and the symbols used in this book are explained fully in Chapter 3.

Obviously, many persons contribute to the development of any book and there is no way we could acknowledge them all. Our primary thanks must go to our families, to whom it must seem as though we will never stop writing and revising books.

TUCSON, ARIZONA

F. J. Hill
G. R. Peterson

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