Two-Stage Class-AB OTA with Enhanced DC-Gain and Slew Rate

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Abstract

This letter proposes a new two-stage class-AB operational trans-conductance amplifier (OTA). In this OTA, the characteristics of class-AB are applied in both of the stages. By increasing the effective trans-conductance of the first stage, DC-gain is improved. Nonlinear current mirror boosts the current of the second stage; Therefore, Slew Rate (SR) is increased. In order to verify the performance of the proposed OTA, some simulations are carried out in a 0.18μm CMOS process in which the supply voltage is 1.8 V. The simulation results indicate 21 dB enhancement in DC-gain and 2.7 times improvement in SR compared to its conventional counterpart. The post-layout and Monte Carlo (MC) simulations show the proposed OTA has better performance than the state of the art designs.

Keywords: Operational Trans-conductance Amplifier; Class-AB OTAs; DC-Gain; Slew Rate; Post-layout Simulation.

1. **Introduction**

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Nowadays, due to increase in applications of switched-capacitor, sample-and-hold circuits, and data converters in electronic circuits, serving of OTAs is necessary as one of the main usable part in their circuit configurations (Akbari, Biabanifarda, Asadi, & Yagoub, 2014; Akbari, Biabanifarda, Asadi, & Yagoub, 2015). The OTAs should have high DC-gain, slew rate (SR), and unity-gain bandwidth (UGBW) while operating with low-voltage and low static power. Achieving these specifications are not viable using class-A OTAs. This is mainly due to the fact that the increasing of SR and UGBW would lead to increase power dissipation, considerably. Some techniques have been proposed in the literature for low-power OTAs. One of these techniques is based on bulk-driven method (Ferreira, Pimenta, & Moreno, 2007; Raikos & Vlassis, 2011; Ferreira & Sonkusale, 2014). The main disadvantage of a bulk-driven MOS device in CMOS technologies is that bulk-source trans-conductance is smaller than the gate-source trans-conductance and may not be sufficient in some cases. Class-AB OTAs can be considered as a better solution for the realization of the above specifications.

Several class-AB OTAs have been suggested in the literatures (Callewaert & Sansen, 1990; Galan, López-Martín, Carvajal, Ramírez-Angulo, & Rubia-Marcos, 2007; Noormohammadi & Hajsadeghi, 2012; Liu & Yang, 2006; Baharudin, Jambek, & Ismail, 2014). A class-AB OTA has been introduced to increase tail current when large input signals are applied (Callewaert & Sansen, 1990). However, due to the extra circuitry, the power consumption has increased drastically. An adaptive-biasing circuit (ABC) based class-AB OTA has been proposed that is suitable for low-voltage operation (Galan, López-Martín, Carvajal, Ramírez-Angulo, & Rubia-Marcos, 2007). The main drawback of this technique is its poor performance in terms of output noise. A class-AB output stage OTA using current boosting method has proposed which enhances both of the SR and UGBW parameters (Noormohammadi & Hajsadeghi, 2012). This method suffers from high static power consumption due to class-A operation of the input stage. A low-voltage, low-power class-AB OTA has been proposed, which is based on the current mirror OTA topology and positive feedback (Liu & Yang, 2006). However, stability of the OTA may encounter difficulties due to variations of process and environmental parameters. A two-stage OTA has been proposed which has high DC-gain (Baharudin, Jambek, & Ismail, 2014). However, SR has not been increased significantly. In this letter, a new two-stage class-AB OTA has been introduced. The results indicate the superiority of the proposed technique in terms of DC-gain and SR compared to the conventional OTA. In Section 2, the proposed OTA is described. The performance evaluations of the OTA and comparison results are presented in Section 3. Finally, Section 4 concludes the letter.

2. Proposed OTA

Figure 1 shows the conventional two-stage OTA that utilizes hybrid-cascode compensation technique (Yavari, 2005). Also, Figure 2 shows the circuit configuration of the proposed OTA. The common-mode feedback (CMFB) circuit is shown in Figure 3. The differential pair in the first stage consists of two matched transistors M_1 and M_2 which are biased by an ABC. Under the conditions in which the differential input is not applied, small quiescent currents would be flowed through M_1 and M_2. However, this current would be boosted when the differential input voltage is sensed by ABC. Based on the aforementioned discussion, the proposed circuit can be classified as a class-AB OTA.
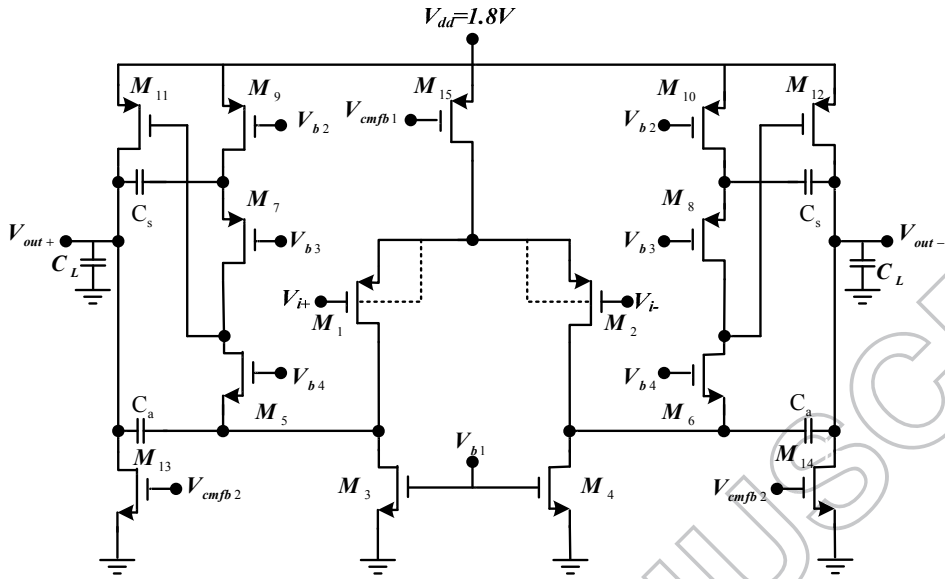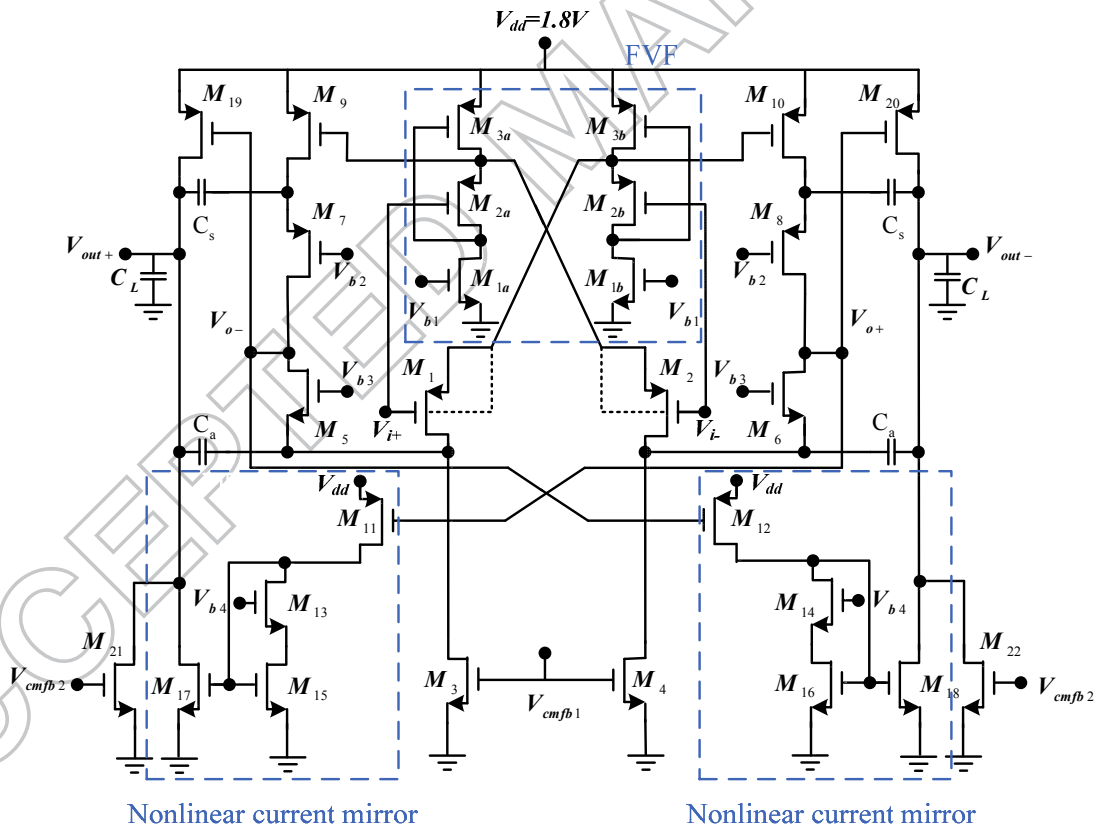
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Figure 1. The conventional OTA.
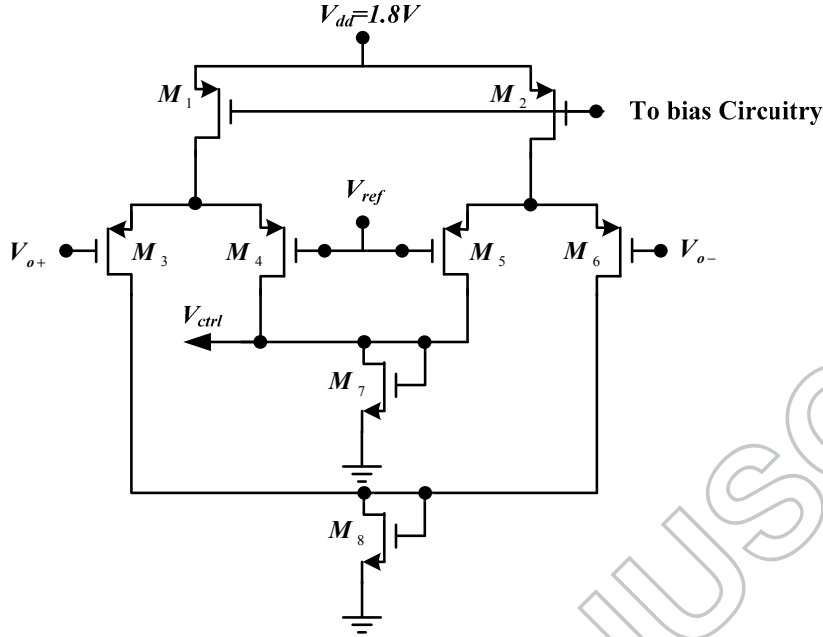

Figure 2. The proposed OTA.

3

Figure 3. Common-mode feedback (CMFB) circuit

The adopted ABC is composed of a modified version of the source follower named as flipped voltage follower (FVF) (Carvajal, Ramirez-Angulo, Torralba, Galan, Carlosena, & Chavero, 2005; Guo, Ho, Kwong, & Leung, 2015; Kim & Lee, 2013). The FVF consists of transistors M_{2a}, M_{2b} and M_{3a}, M_{3b}, in which M_{1a}, M_{1b} act as current sources that provide quiescent current equal to I_B. By neglecting second-order effects, the source-gate voltage of M_{2a} is given by

$$V_{SG2a} = \sqrt{\frac{2I_B}{_pC_{ox}(W/L)_{2a}}} + \left|V_{th,p}\right|_{2a} \tag{1}$$

where $V_{th,p}$ is the threshold voltage of PMOS transistor. By considering $V_{G9} = V_{SG2a} + V_{CMi1}$, where V_{CMi1} is the input common-mode voltage of the first stage, the current through M_9 can be obtained. The source-gate voltage of M_2 is given by $V_{SG2} = V_{SG2a}$, therefore, the current through M_2 is calculated. The voltage V_{O-} is determined by CMFB1; hence, the current through M_{19} is found.

By applying the input signal, the current flowing in one of the differential pair transistors increases. For example, consider a condition in which V_{i+} and V_{i-} increases and decreases, respectively. Upon this, the source voltages of M_1 and M_2 are decreased and increased, and their drain currents would be decreased and increased, respectively. Source of M_2 is connected to the drain of M_{3a} and to the gate of M_9. Also, Source of M_1 is connected to the drain of M_{3b} and to the gate of M_{10}. This architecture realize the class-AB operation for the active load transistors M_9 and M_{10} that are associated with the common-gate transistors M_5 and M_6. By applying the input signal to the OTA, this

4

signal would also appear at the gate-source of M_9 and M_{10} by means of FVF. Therefore, the trans-conductance of the input stage is increased from $g_{m1,2}$ to $g_{meff} = g_{m1,2} + g_{m9,10}$ which enhance the DC-gain. Increasing the input stage trans-conductance can also reduce the total input-referred noise voltage as follows:

$$\overline{V_{ni,\text{prop}}^2} \approx \left(\frac{g_{m1,a}}{g_{meff}^2}\right) \times 4kT + \left(\frac{g_{m1}}{g_{meff}}\right)^2 \times \overline{V_{ni,conv}^2} + \frac{g_{m3}}{g_{meff}^2} \times 4kT \tag{2}$$

where $\overline{V_{ni,conv}^2}$ denotes the total input-referred noise voltage of the conventional OTA.

FVF-based nonlinear current mirrors have been used for the output active loads that are composed of transistor sets $(M_{11}, M_{13}, M_{15}, M_{17})$ and $(M_{12}, M_{14}, M_{16}, M_{18})$. The gates of M_{11} and M_{12} are connected to the nodes V_{o+} and V_{o-}, respectively. The transistors M_{15} and M_{16} are biased close to the triode region so that their drain-source voltages would be a bit higher than $V_{DS,sat}$. Consider a condition in which input voltages V_{i+} and V_{i-} are increased and decreased, respectively. Then, voltages of the nodes V_{o-} and V_{o+} are decreased and increased, respectively. The current through M_{12} increases by decreasing the voltage of the node V_{o-}. Then the gate-source voltage of M_{14} and the drain-source voltage of M_{16} are increased and decreased, respectively. Thus M_{16} is pushed into the triode region. As a result, a large voltage variation is produced across the gate-source of M_{16} that can be expressed as below:

$$I_{16} = {}_{16}(V_{GS16} - V_{th,n})V_{DS16} \tag{3}$$

where ${}_{16} = {}_n C_{ox}(W/L)_{16}$ and $V_{th,n}$ is the threshold voltage of NMOS transistor. A large gate-source voltage variation of M_{16} would boost the current of the active load M_{18}. This current can be obtained by equation (4) as long as it remains in saturation region.

$$I_{18} = \frac{{}_{18}}{2}\left[\frac{\frac{{}_{12}}{2}\left(V_{DD} - g_{meff}\frac{V_{id}}{2}R_{o1} - V_{CMO1} - V_{th,n}\right)^2}{{}_{16} \times V_{DS16}}\right]^2 \tag{4}$$

where V_{CMO1} is the common-mode output voltage of the first stage, and R_{o1} denotes the resistance of node V_{o-}. From (4) it is clear that for a large V_{id} the output current increases with V_{id}^4, that would enhance the current boosting provided by the Class-AB, quadratically.

3. Simulation Results
In order to verify the performance of the proposed OTA compared to the conventional one, some simulations are carried out. Both of the competitors are designed in a 0.18 μm CMOS process with 1.8V supply voltage. Supply voltage, load capacitor, phase margin,

and power dissipation are identical for both OTAs. Currents allocations to MOSFETs used in the proposed OTA are reported in Table 1. *Gm* versus differential input voltage for both of the proposed and conventional OTAs are demonstrated in Figure 4. The results show that the *Gm* of the proposed OTA is higher than the conventional OTA.

The Bode diagrams of the competitors are shown in Figure 5, indicating 21 dB DC-gain improvement in schematic level simulation. UGBW and phase margin of the proposed OTA are 270 MHz and 65°, respectively. Complete OTA specifications along with a comparison to the conventional OTA are summarized in Table 2. As seen from the results, SR of the proposed OTA has been enhanced 2.7 times compared to its conventional counterpart. Moreover, the total input-referred noise voltage of the proposed OTA is smaller than the conventional design. The physical layout of the both OTAs is shown in Figure 6. As a drawback, the layout area of the proposed OTA is increased by the factor of 1.2 compared to the conventional one. This is mainly due to larger compensating capacitors in the proposed OTA for achieving equal phase margin compared to conventional OTA.

Figure 7 shows the Monte Carlo (MC) histograms of the proposed OTA comprising of 10000-run simulations, and the results are summarized in Table 3. The results show that the variations in OTA specifications are relatively low.

Post-layout simulation results are compared with some other methods in Table 4. The proposed OTA shows the small value for layout area compared to the most existing methods. Moreover, the proposed OTA has the highest DC-gain, at least 19 dB more than the other solutions. In order to compare the other performance parameters, the traditional couple of figure of merits in (5), (6) which for a given load show a trade-off between speed performance and total bias current (I_T) are utilized (Grasso, Palumbo, & Pennisi, 2006; Grasso, Palumbo, & Pennisi, 2007).

$$FOM_S = \frac{UGBW \cdot C_L}{I_T} \tag{5}$$

$$FOM_L = \frac{SR \cdot C_L}{I_T} \tag{6}$$

As can be seen from Table 4, the proposed OTA has proper values for both of FOMs and FOM_L.

Table 1. Currents allocations to MOSFETs.

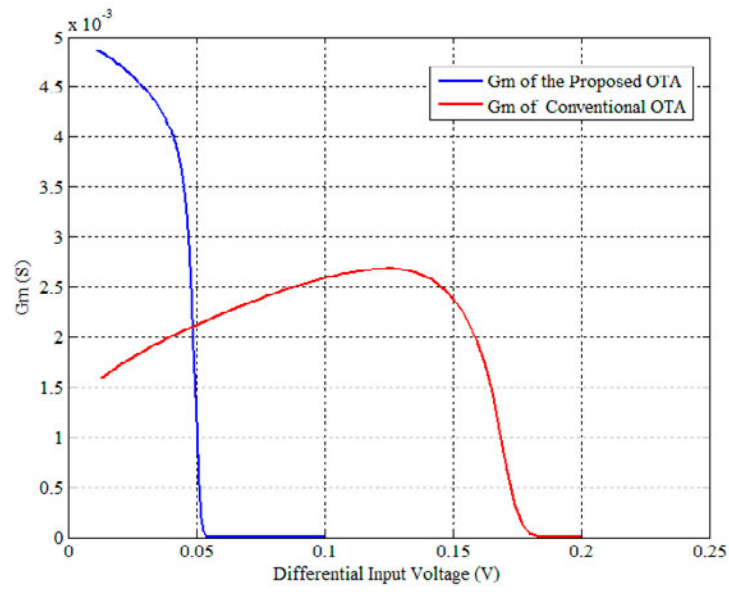| Device	Current Value (μA)
M_1	128
M_{1a}	114
M_9	214
M_{11}	98
M_{19}	255

6

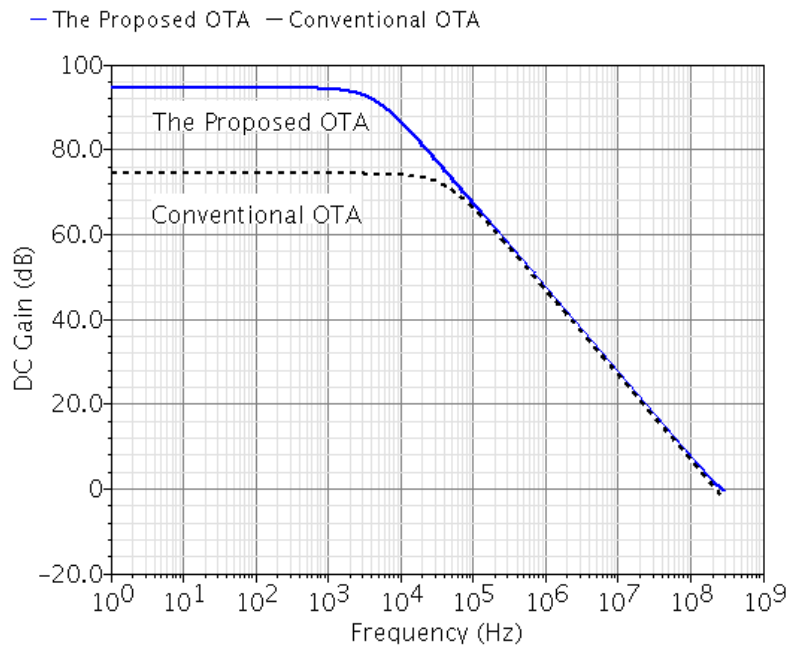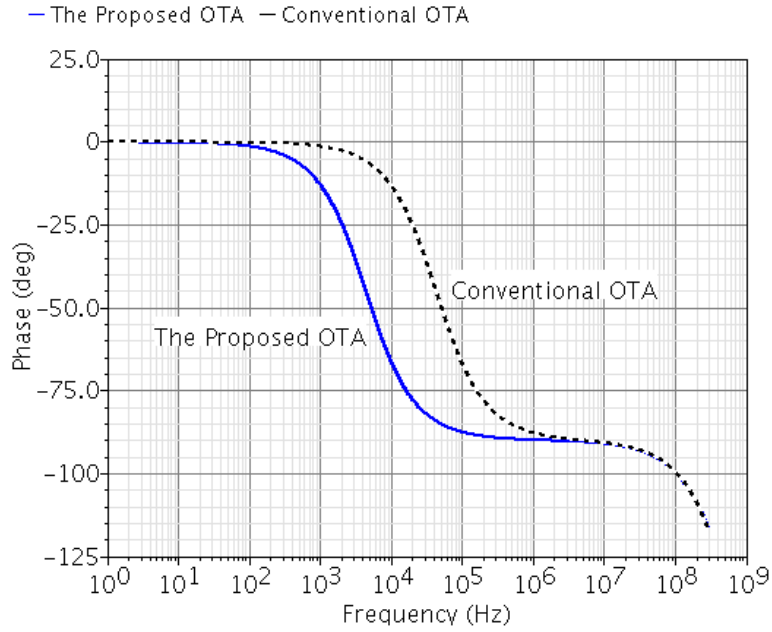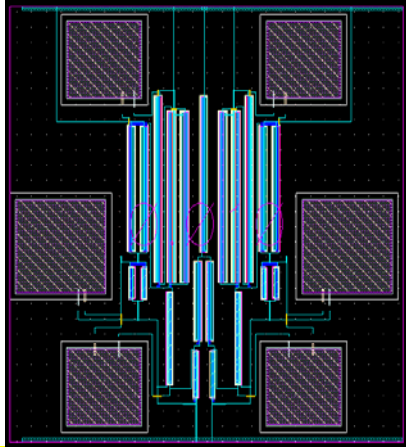**Figure 4.** *Gm* versus differential input voltage for both OTAs.

Figure 5. Bode diagrams of the OTAs.

Table 2. Specifications of the proposed and conventional OTAs.

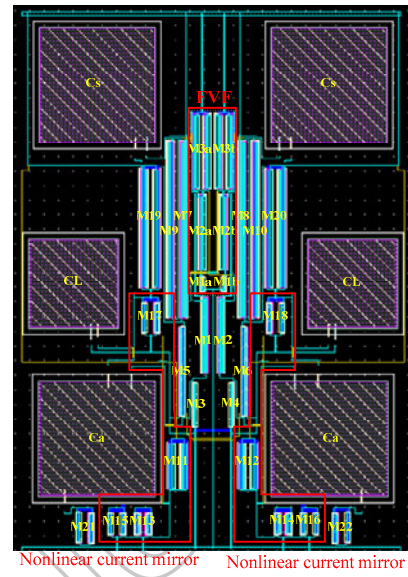| Specification	Conventional OTA			Proposed OTA		
	TT(27°C)	FF(-40°C)	SS(90°C)	TT(27°C)	FF(-40°C)	SS(90°C)
Technology	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm
Supply Voltage	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
DC-Gain (dB)	74	69	71	95	86	96
Input-Referred Noise@100kHz ($\mu V/\sqrt{Hz}$)	0.55	0.44	0.95	0.29	0.24	0.35
Layout Area	131μm×142μm	131μm×142μm	131μm×142μm	131μm×164μm	131μm×164μm	131μm×164μm
Output Voltage Swing (peak to peak) (V)	2.8	2.8	2.8	2.8	2.8	2.8
Phase Margin ($^\circ$)	68	64	78	65	63	67
Power Dissipation (mW)	2.9	4.3	1.8	2.9	3.9	2.1
Slew Rate (V/μs)	221	398	120	595	776	399
UGBW (MHz)	220	368	91	270	390	180
C_L (pF)	1	1	1	1	1	1

Figure 6. Physical layout of **(a)** the conventional and (**b**) proposed OTAs.
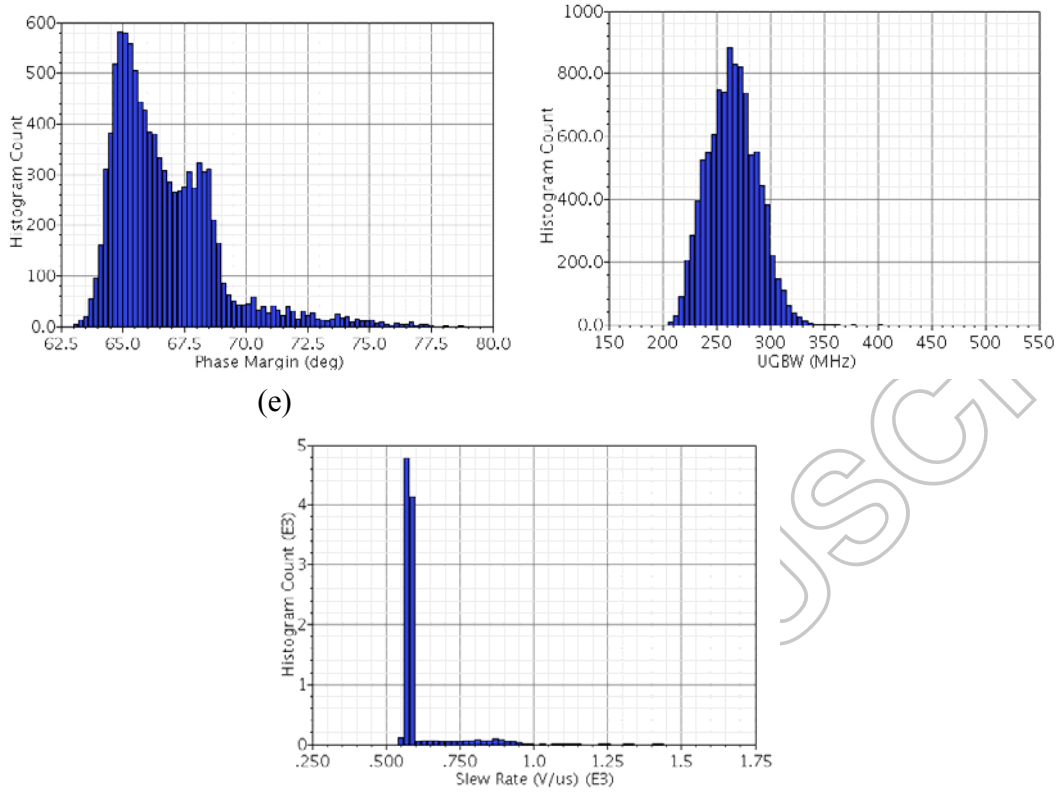
(e)
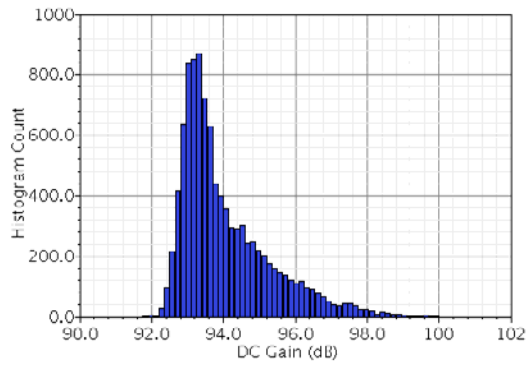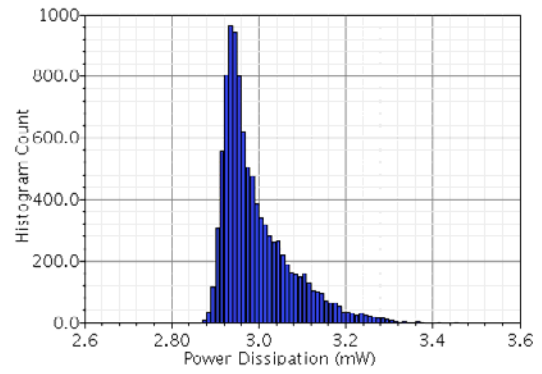
Figure 7. Histogram of Monte Carlo Simulation. (a) DC Gain, (b) Power Dissipation, (c) Phase Margin, (d) UGBW, (e) SR.

Table 3. The Monte Carlo Analysis of the Proposed OTA.

Specification	Mean Value	Standard Deviation
DC Gain (dB)	94.1	1.2
Power Dissipation (mW)	2.9	0.079
Phase Margin ($^\circ$)	66.7	2.1
UGBW (MHz)	265.1	22
Slew Rate (V/µs)	599	58

Table 4. Performance Comparison of the Proposed OTA and the Existing Methods.

	This work	Yavari. (2005)	Ferreira, et al. (2007)	Raikos, et al. (2011)	Ferreira, et al. (2014)	Galan, et al. (2007)	Baharudin, et al. (2014) [b]
Technology	0.18µm	0.18µm	0.35µm	0.18µm	0.13µm	0.5µm	0.13µm
Supply Voltage (V)	1.8	1.8	0.6	1	0.25	1	2.5
DC-Gain (dB)	93	72	69	64	60	30	74
Input-Reffered Noise@100kHz ($\mu v/\sqrt{Hz}$)	0.31	0.58	--	--	--	144	--
Layout Area (mm^2)	0.021	0.018	0.060	0.063	0.083	0.011	--
Differential Output	2.8	2.8	--	--	--	--	2.4

Swing (peak to peak) (V)							
Phase Margin (degree)	65	66	65	45	53	90	62
Power Dissipation (mW)	3	3	0.00054	0.13	0.000018	0.08	1.3
Slew Rate (V/µs)	494	190	0.015	0.7	0.0007	0.35	47.9
UGBW (MHz)	216	177	0.011	2	0.002	0.2	0.02
Loading Capacitance (pF)	1	1	15	1	15	80	3
Operating Mode[a]	SI	SI	SUB, BD	SI, BD	SUB, BD	SI	SI
$FOM_S = \dfrac{MHz.pF}{mA}$	135	111	183	15	417	200	0.115
$FOM_L = \dfrac{V.pF}{\mu s.mA}$	309	119	250	5	146	350	276

[a]SUB: subthresold; BD: bulk driven; SI: strong inversion.

[b]Only Schematic level simulation

4. **Conclusion**

In this letter a new two-stage class-AB OTA in a 0.18 µm CMOS process with a 1.8 V supply voltage has been presented. The proposed OTA was based on the simultaneous application of class-AB operation in both of the stages. In order to evaluate the effectiveness of the proposed method, several simulation scenarios have been performed. The results indicated the superiority of the proposed OTA in terms of DC-gain and SR compared to the conventional OTA with the cost of a little increase in the layout area.

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1) Reviewer(s)' Comments to Authors:
Please note that your paper should be formatted according to the Journal's rules, in particular please use APA style for the references.
ANS. The manuscript has been modified.

2) there are no explain about layout fig. compare the schematic, please. Mark the FVF and nonlinear current mirror part at layout fig.
ANS. Thank you for your valuable comment. Please consider the Figure 6(b).
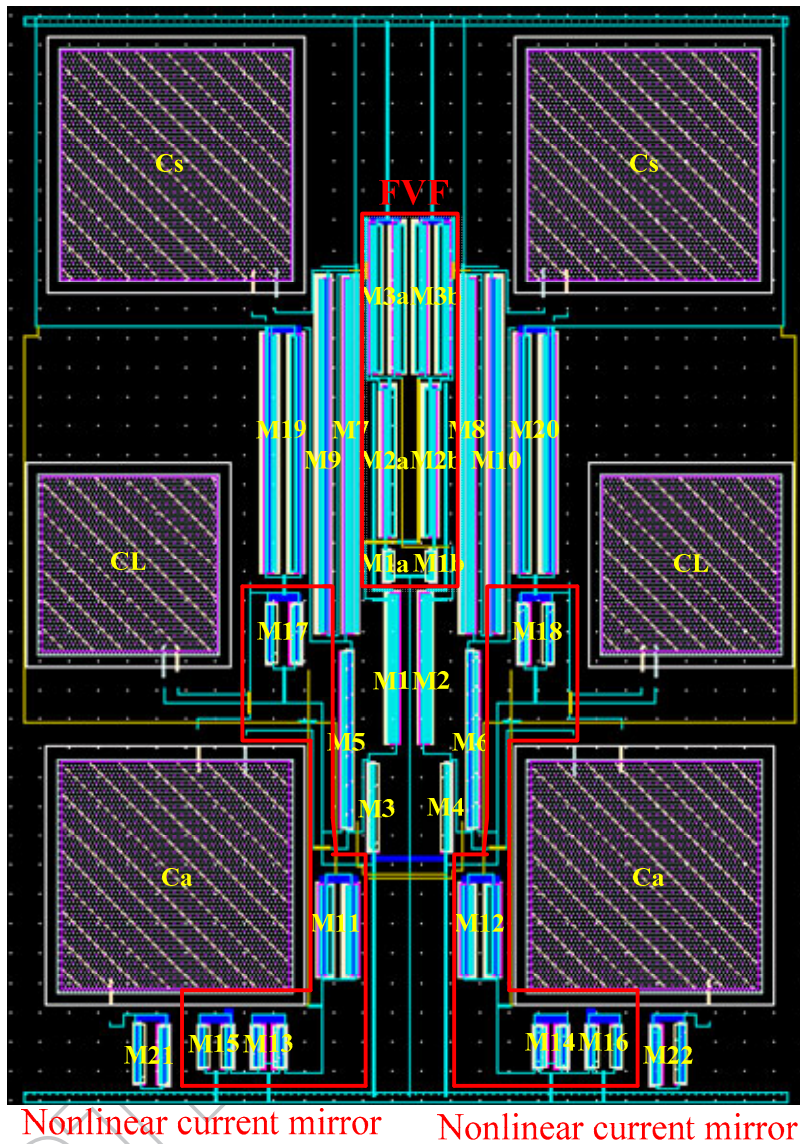
3) Please considering ref. papers.
A Capacitorless LDO Regulator With Fast Feedback Technique and Low-Quiescent
Current Error Amplifier, IEEE Transactions on Circuits and Systems II: Express Briefs
(Volume:60, Issue: 6),Young-il Kim.
ANS. We would like to thank the reviewer for bringing this paper to our attention. The
manuscript has been modified according to the above comment.