

High-speed low-power common-mode insensitive dynamic comparator

Junfeng Gao, Guangjun Li and Qiang Li

A new structure single-stage dynamic comparator with a large input common-mode range is proposed. The proposed comparator is compared with previous dynamic comparators. With same size input transistors and load capacitance, it is more than 1.2 times faster with <80% power consumption. Also, the input-referred noise and offset are no more than the previous comparators.

Introduction: Comparators are crucial circuits in analogue-to-digital converters (ADCs) to convert analogue signals into digital form. Without intrinsic gain and error correction, the performances of ADCs are dominated by comparators, especially in the case of successive-approximation resistor ADCs, which require intensively low noise, low-power and high-speed operation of comparators to achieve high speed and high resolution. In [1] a fully double-tail dynamic comparator with fast latching speed and static power free feature is introduced. The number of cascading transistors from supply to ground is limited to three transistors to enhance the comparison speed. Following the double-tail comparator, faster dynamic comparators with shared current between the first stage and the latch are analysed in [2, 3]. In both works, extra transistors are adopted to connect the latch and ground to accelerate the latching speed. However, static power is dissipated in either the reset cycle or the comparison cycle for [2, 3]. Compared with these dynamic comparators, this Letter proposes a new structure single-stage dynamic comparator achieving the fastest speed, lowest common-mode sensitivity and power consumption with moderate input-referred noise and offset.

Circuits implementation: As illustrated in Fig. 1, the double-tail comparator in [1] adopts a fully dynamic preamplifier in the first stage to minimise static power consumption. M10 and M11 provide signal amplification to the latch before regeneration. After turning on M9, D_{ip} and D_{in} are drawn to the ground at different speeds with respect to differential inputs. This difference is then regenerated and stored by the latch. The speed and offset of the preamplifier are limited by M9 and the speed of the latch is dominated by the slower P-type MOS (PMOS) M12.

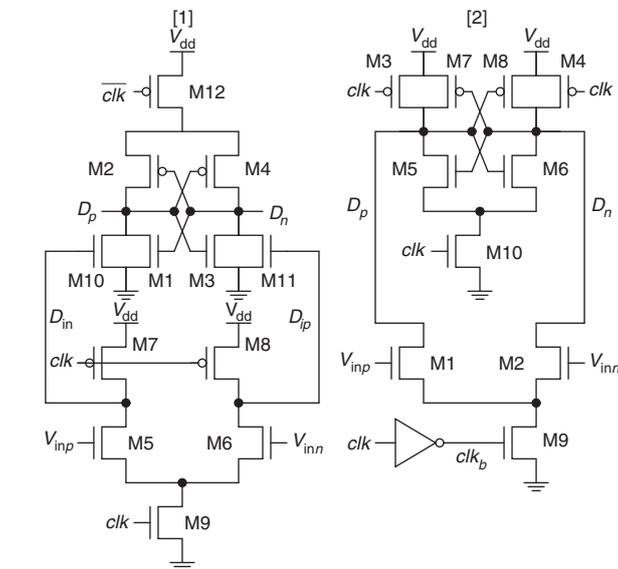


Fig. 1 Dynamic comparator structures – doubletail comparator

The comparator in [2] introduces analogue signal through current rather than voltage from the preamplifier to the latch. A first-stage preamplifier is formed by M1–M4 and biased through M9. The preamplifier output is directly connected to the latching nodes to reduce the overall amplification and regeneration delays. However, this structure increases the load capacitance at the output nodes. The latch in [3] is a single-stage comparator. clk_2 is the delayed signal of clk_1 which can reduce the input-referred noise by maintaining M1 and M2

saturated with $clk_1 = 1$ and $clk_2 = 0$. With $clk_2 = 1$, regeneration starts with speed acceleration of M12 and M13. However, when the preamplifier is functional during the reset or comparison phase in [2, 3], static power is consumed. The inverter input structure of [3] can enlarge the input common-mode range to a lower voltage but its latch can be disabled when T_{ip} and T_{in} comes to V_{dd} .

To realise fast comparison and avoid static power consumption, a new single-stage dynamic comparator structure is proposed, see Fig. 2. The analogue signal is also delivered to the latch in the current mode. M10 and M11 reset output nodes D_p , D_n to V_{dd} and the back-to-back inverters (M6–M9) start comparison after M3 is turned on with M10 and M11 turned off by clk_1 . clk_2 is also the delayed signal of clk_1 so that M4 and M5 are turned on later to accelerate the regeneration speed.

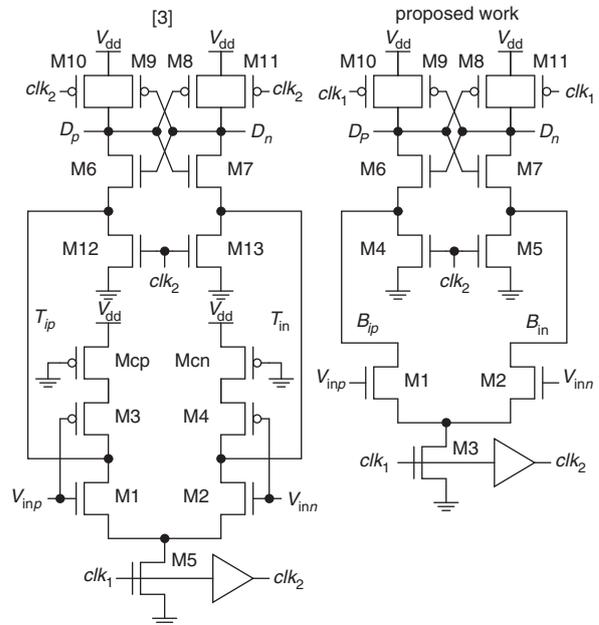


Fig. 2 Dynamic comparator structures – new single-stage comparator

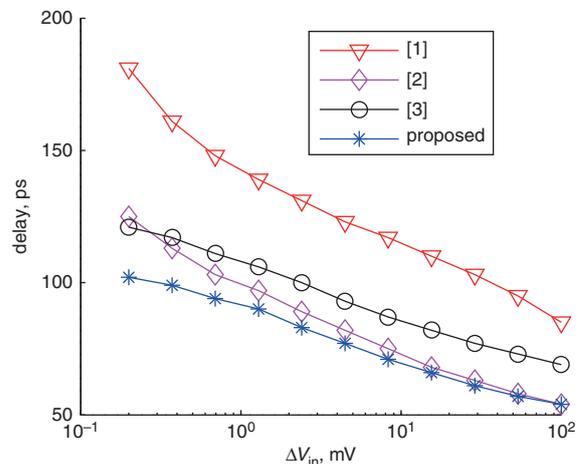


Fig. 3 Simulated delays against differential input voltage

Performances of comparators: To compare the performance of all four comparators, they are carefully designed in a 0.13 μm CMOS technology with the same size input transistors and 20 fF load capacitance. Abbas *et al.* [2] and Chan *et al.* [3] and this Letter share the same sized and same structured dynamic latch. The delays of the four comparators at output nodes D_p , D_n are simulated at 1.25 GHz frequency with $V_{dd} = 1.2$ V and $V_{cm} = 0.6$ V. The delay is measured at 0.7 V for the P-type latch in [1] and 0.5 V for the N-type latch in [2, 3] and for this Letter. The simulated delays are illustrated in Fig. 3. The proposed comparator has the fastest comparison speed with acceleration of M4 and M5, which is 1.6 times that of [1] and 1.2 times that of [3]. The reason is that the PMOS is slower in [1] and regeneration starts after $clk_2 = 1$ (not $clk_1 = 1$) for [3]. The delay sensitivity to input (delay/

$\log(\Delta V_{in})$) of each comparator is compared in Table 1. The proposed comparator has the fastest comparison speed with the smallest delay sensitivity to input.

Table 1: Performance comparisons with input common-mode at V_{cm}

	[1]	[2]	[3]	Proposed
Delay sensitivity, ps/dec	35.5	24	19.3	17.8
Input-referred noise, μV	257	770	434	435
Offset σ , mV	6.76	13.3	8	7.78
Power consumption, mW	0.82	1.14	0.76	0.6

The workable common-mode ranges for the four this comparators are shown in Fig. 4, with differential input $V_{in} = 0.5$ mV. The power dissipations with respect to common-mode voltage are drawn in Fig. 5. The largest common-mode variation endurance and lowest power consumption can be achieved by the proposed comparator. The power consumption of the proposed comparator is the lowest among the four comparators, which is about 80% of the power of [1, 3] (power outside the workable common-mode range is ignored). In [2] much higher power is spent because of the static current in the amplification phase. In [3] it is more stable around $V_{dd}/2$ and the low voltage because of the PMOS differential inputs with higher power consumption. Schinkel *et al.* [1] has better performance at a higher common-mode voltage but consumes more power because of the two stacked PMOS in the latch.

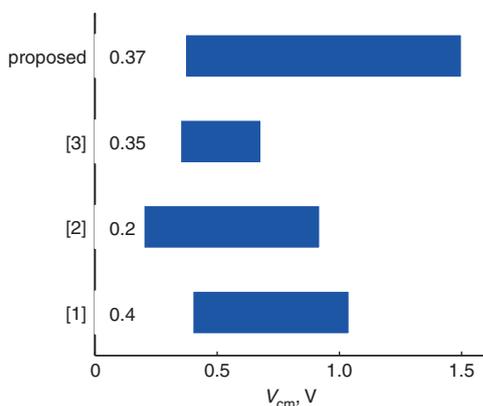


Fig. 4 Common-mode sensitivity of comparators

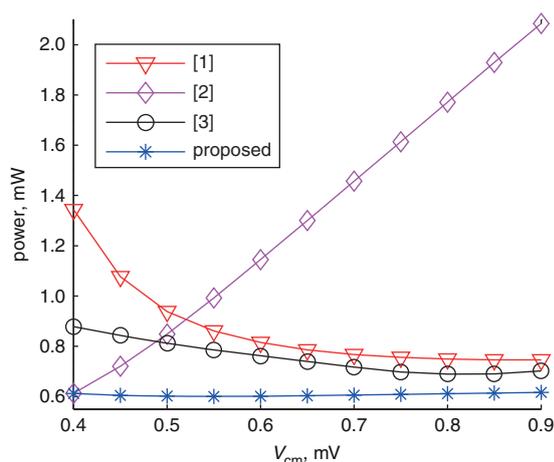


Fig. 5 Power consumption of comparators against common-mode variation

The simulated input-referred noise and offset σ are demonstrated in Table 1. The input-referred noise and offset of the proposed comparator

is only larger than [1] due to the faster comparison speed and low power consumption. However, the overall performance of the proposed comparator is better than in [1–3] in terms of speed, power and workable common-mode range.

Conclusion: In this Letter, a new structure single-stage dynamic comparator is proposed. The proposed comparator achieves the fastest comparison speed with lowest power dissipation compared with the conventional dynamic comparators in [1–3]. The input-referred noise and offset of the proposed comparator are larger than [1] but no more than [2, 3]. The workable common-mode range for the proposed comparator is the largest among all the analysed dynamic comparators which even covers voltage beyond the power supply. Considering the overall performance of the dynamic comparator, it is more efficient for adoption in high-speed data conversion.

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One or more of the Figures in this Letter are available in colour online.

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