A 0.25 μm InP DHBT 200 GHz+ Static Frequency Divider

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***Abstract*—Static frequency dividers are widely used technology performance benchmark circuits. Using a 0.25 μm 530 GHz f_T/600 GHz+ $f_{\max}$ InP DHBT process, a static frequency divider circuit has been designed, fabricated, and measured to operate up to 200.6 GHz [1]. The divide-by-two core flip-flop dissipates 228 mW. Techniques used for the divider design optimization and for selecting variants to maximize performance across process changes are also discussed.**

***Index Terms*—Digital, divider, frequency, HBT, high speed, InP, static.**

I. Introduction

As HIGH-SPEED communication channel throughput and performance needs continue to evolve so do the technologies used to implement the various system building blocks. Static frequency dividers are widely used as a circuit performance benchmark or a figure-of-merit indicator to gauge a particular device technology's ability to implement high-speed digital and integrated high performance mixed-signal circuits. The InP double heterojunction bipolar transistor (DHBT) technology, characterized by high electron mobility in the InGaAs base, high g_m, and high breakdown voltage, remains a strong competitor for use in ultra-high performance analog/mixed-signal and digital circuits. InP bipolar transistors can achieve higher bandwidth than Si devices with less aggressive scaling and much simpler as well as less expensive fabrication processes. Recent InP DHBT technologies have demonstrated remarkable high-speed performance from transistors with sub-micron features achieving >400 GHz f_T and $f_{\max}$ [2]–[7] and divider operation up to the 150 GHz range [8]–[12]. Other device technologies such as SiGe [13]–[15] and CMOS [16] have reported >95 GHz and 66 GHz static frequency divider operation, respectively. Fig. 1 highlights notable static frequency divider performance achievements over the last 10 years in various device technologies.

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We report measured results for a 200.6 GHz static frequency divider demonstration circuit fabricated in a highly scaled 0.25 μm InP DHBT process with an $f_T = 530$ GHz and $f_{\max}$ in excess of 600 GHz. To the author's knowledge, this is the highest reported frequency of operation for a static frequency divider.

II. Technology

The divider demonstration circuit was fabricated using Northrop Grumman Corporation's 0.25 μm InP DHBT process. The advanced InP DHBT process has been developed to provide device and interconnect scalability with an emphasis on manufacturability and yield [17]–[19]. Aggressive emitter mesa scaling is achieved using a plasma etch process. The emitter size is defined by a combination of photolithography and nitride masking followed by semiconductor dry etches. The emitter formation is terminated by a short selective wet etch to remove plasma damage. Minimum InP emitter undercut for reduced base access resistance is achieved by minimizing the wet etch time since most of the emitter height is produced by dry etching. The emitter mesa is followed by a self-aligned base metallization process. Base metal and mesa layouts are designed to produce minimum base-collector capacitance (C_{jc}) while maintaining low base resistance values. A thin dielectric layer is immediately deposited after base metal lift-off to protect and passivate the emitter junction. The less critical base and isolation mesas are produced using full wet etch process, with dry etch being considered as a future replacement to achieve further compaction. The device contact via process is implemented with a highly selective dielectric etch that enables device scaling down to 0.25 μm emitter widths at no manufacturing penalty. A cross section of a super-scaled 0.25 μm emitter HBT is shown in Fig. 2. The dotted line represents physical dimensions of our previous ultra-high-speed device generation [2].

The remaining active and passive element process steps can be found in [15]. The technology offers Schottky diodes, 0.19 fF/μm^2 MIM capacitors, and precision thin film resistors of 20 and 100 $\Omega/\square$. The fabrication of integrated circuits is completed by a multi-level interconnect process presented in Fig. 3 with four plated Au metal layers and low-k benzocyclobutene (BCB) as the interlayer dielectric between metallization.

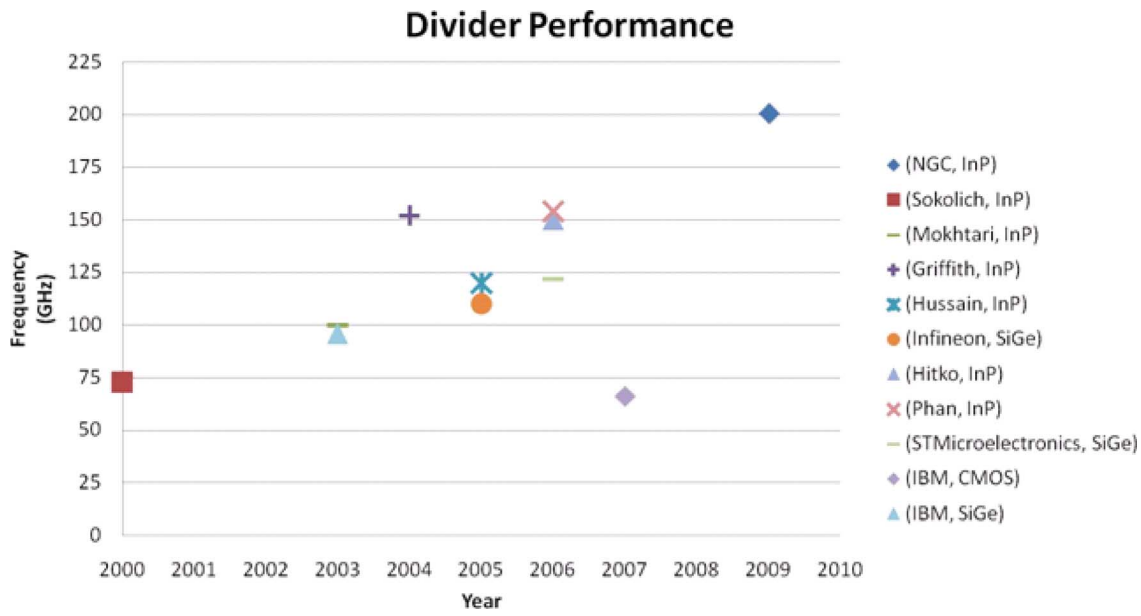

Fig. 1. Divider performance highlights over the last 10 years.

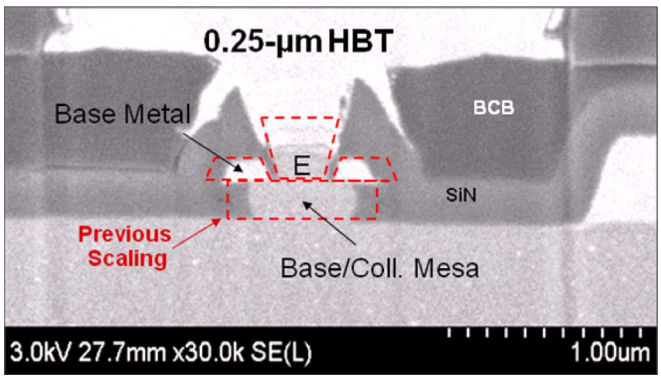

Fig. 2. SEM cross-sectional SEM image of InP HBT with a 0.25 μm base/emitter junction. The dashed boundaries correspond to the physical dimensions from NGAS's previous high-speed device generation.

A. Epitaxial Details

Epitaxial layers have been aggressively designed for ultra high-speed performance. The MBE-grown DHBT structure uses an n-type doped ($>5 \times 10^{17}$ cm^{-3}) InP emitter terminated with an In-rich, heavily doped InGaAs cap layer for low emitter contact resistance. Overall emitter height has been reduced for improved emitter access resistance. The InP emitter design simplifies device fabrication as it allows for selective wet etching to the base semiconductor. The 220 Å base layer uses a compositionally-graded InGaAs material doped p$^+$ (8×10^{19} cm^{-3}) to obtain low base resistance. The total InP collector layer thickness is 1200 Å, and its doping level (8×10^{16} cm^{-3}) is adjusted to support increased current density suitable for high-speed digital applications. Additional collector profiles have been developed for other digital or mixed-signal applications. Process options include thicker InP collector (up to 5000 Å) that optimally support maximum large signal analog performance at lower current densities.

B. Device Results

The common-emitter I-V plot for a 0.25×4 μm^2 emitter area DHBT using a thinned collector of 1200 Å is shown in Fig. 4. The breakdown voltage (BV_{CEO} at 10 μA/μm^2) is slightly over 4 V, while increased doping level in the collector allows for non-blocking operation well in excess of 10 mA/μm^2. The common-emitter current gain (β) for this device is 30, as shown in the Gummel characteristics from Fig. 5. Higher current gain value >50 can be achieved for the same emitter size with special base/emitter heterojunction bandgap engineering and the use of a sidewall process.

DC-110 GHz S-parameter measurements have been obtained using an HP 8510XF and on-wafer TRL calibration methods. Extrapolations from RF gains were made without de-embedding techniques. Fig. 6 shows the RF performance characteristics from a 0.25×4 μm^2 emitter area device, while DC biased with $V_{CB} = 0.4$ V and collector current density (J_C) of 13 mA/μm^2. Extrapolated f_T and $f_{\max}$ values versus J_C are plotted from the same 0.25×4 μm^2 device in Fig. 7, with simultaneous peak $f_T = 530$ GHz and $f_{\max}$ in excess of 600 GHz. MAG/MSG of 15.5 dB is measured at 100 GHz.

III. Design and Optimization

The divider design effort was accomplished in parallel with the InP DHBT device development. Therefore, only extrapolated models were available for simulation and design work before fabrication. Novel simulation optimization techniques were used in order to accommodate device uncertainty due to epitaxial and device layout variations as well as modeling inaccuracies to maximize the chances for a first pass success.

The divider architecture consists of several current-mode logic (CML) circuit stages which were highly optimized to obtain peak performance. Peak divider performance was achieved by maximizing input drive power and minimizing the effective

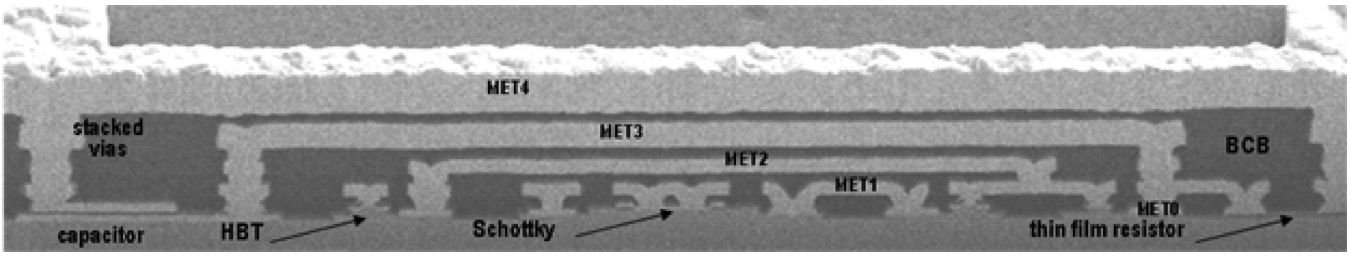

Fig. 3. SEM cross-sectional image of the advanced InP DHBT technology, including 0.25 μm transistors and a four-level interconnect.

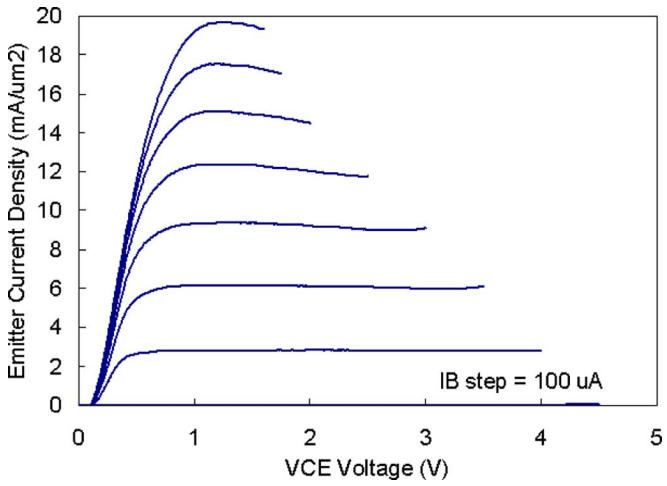

Fig. 4. Common-emitter I.V. characteristics from a 0.25 $\times$ 4 μm^2 InP DHBT using a 220 Å base and a 1200 Å collector.

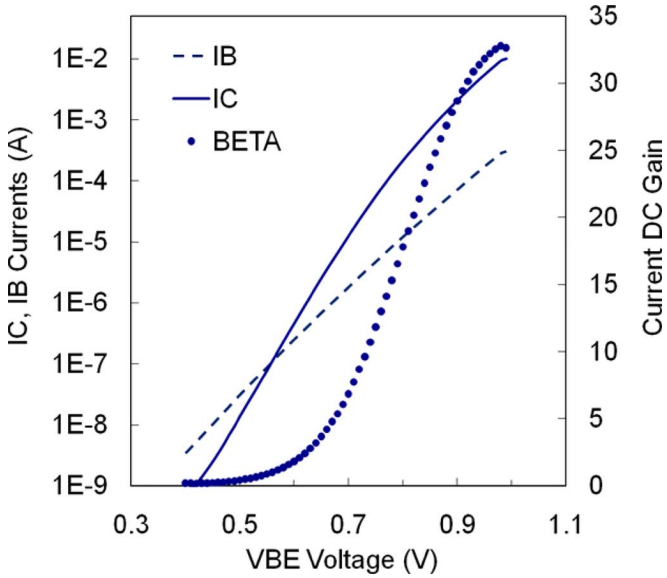

Fig. 5. Gummel characteristics from a 0.25 $\times$4 μm^2 InP DHBT using a 220 Å base and a 1200 Å collector.

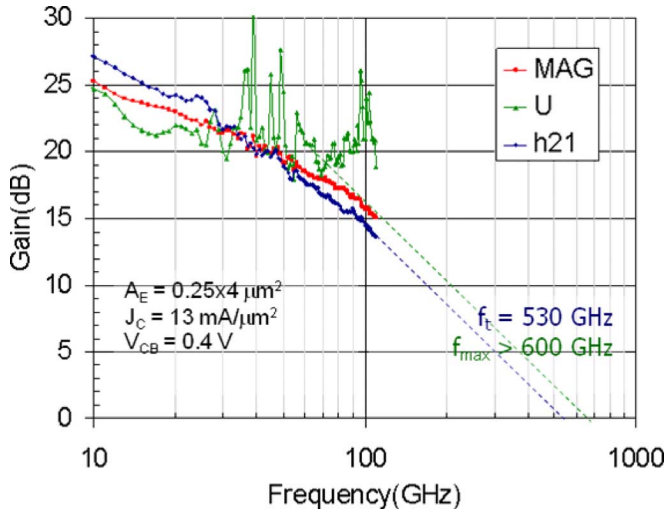

Fig. 6. Extracted RF gains h21, U, and MAG/MSG from S-parameters from a 0.25 $\times$ 4 μm^2 InP DHBT near peak f_T bias point.

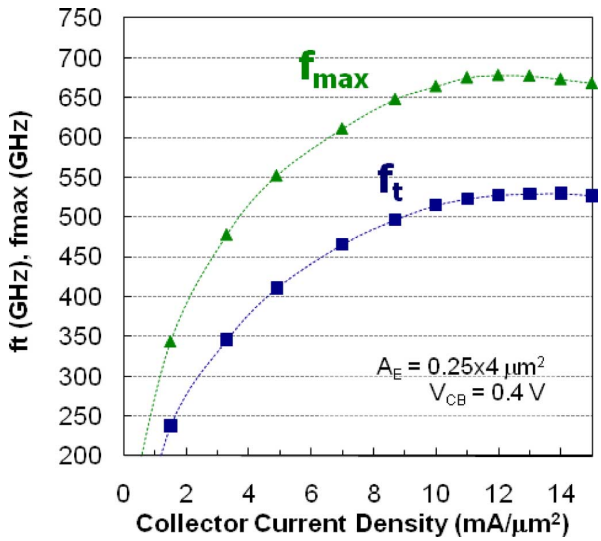

Fig. 7. f_T and $f_{\max}$ extrapolated frequencies versus collector current density from a 0.25 $\times$ 4 μm^2 InP DHBT.

divider output feedback time constant. The circuit stages shown in Fig. 8 consist of front-end bias circuitry, a frequency divider core, and output gain buffers. The demonstration circuit input and output are single-ended interfaces.

A. *Front-End Bias Circuitry*

The front-end of the divider shown in Fig. 9 simultaneously provides the on-chip 50 Ω termination and the bias to the divider circuitry, with no need for intermediate input gain stages

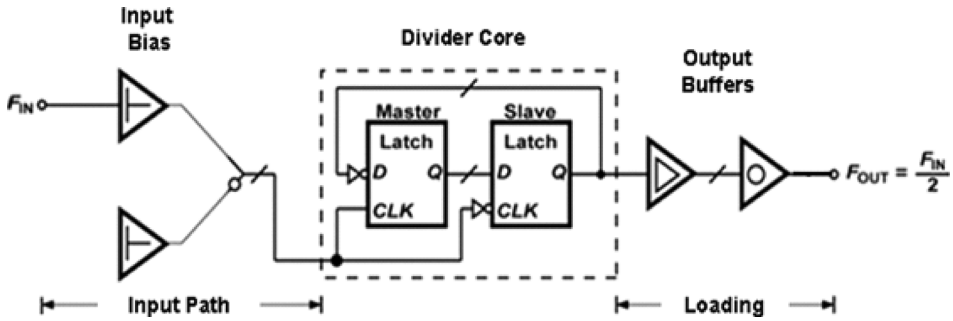

Fig. 8. Top level block diagram.

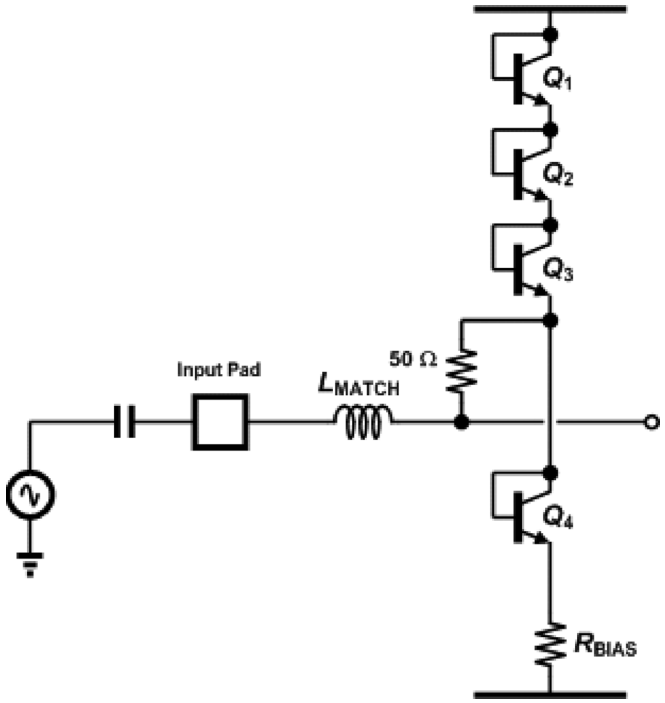

Fig. 9. Input bias circuit diagram.

or impedance transformations which could limit the input power to the divider. The complementary side bias network was not brought out to bond pads. Series diodes and resistors create the necessary level shifting to provide the voltage bias to the lower differential pair inputs of the latches in the divider core. An ultra-broadband matching network using a small micro-strip inductor to effectively tune out the input capacitance of the divider latches and on-chip bond pad was designed to enable maximum input power drive. Simulations showed the input matching network has better than 10 dB return loss across the entire divider frequency of operation (Fig. 10).

B. Frequency Divider Core

The frequency divider core is implemented using a master–slave flip-flop with an inverted output feedback configuration illustrated in Fig. 11. The master–slave latches use 0.25×3 μm^2 devices biased to $\sim$ 14 mA/μm^2 with a -6 V supply. Emitter followers using 0.25×6 μm^2 devices were inserted to provide the impedance transformation for the inductively peaked latch loads and were biased with a -2.8 V supply. The inductive peaking was implemented using a transformer style metal structure (Fig. 12) which directs the differential current in the load to flow in the same direction in adjacent metal conductors increasing the amount of inductance that could be achieved per unit length. As a result more compact inductors with higher Q's could be built to provide "peaking" compensation in the divider feedback path. For the given architecture an optimized inductively peaked latch load and a highly compacted divider layout were necessary to minimize the effective output time constant of the divider feedback path.

The inductively peaked latch load optimization was performed using an automated binary search algorithm to find the maximum frequency of operation for a range of resistances and inductances. The result of the simulation is a divider performance contour plot shown in Fig. 13. As can be seen from the topological plot of one example variant, the peak divider performance occurs at an apex that is near a region of minimized low frequency feedback gain (small resistance) and instability or non static operation (large inductance to resistance ratios). The delicate balance between having just enough low and high frequency feedback gain for broadband operation is the design challenge for achieving continuous frequency division up to the maximum frequency of operation. It is interesting to note that circular bands exist around the apex where it is possible to achieve a certain maximum frequency of operation with more than one combination of resistance and inductance; however, there is only one optimal value of resistance and inductance at the apex, which represents the absolute maximum frequency for static operation. In order to account for process and modeling uncertainty, variants with different combinations of resistance and inductance around the apex were also fabricated. The measured divider reported in this work had an optimal resistance of 30 Ω and inductance of 22.5 pH.

Variants of the divider design with different combinations of optimized load resistance and inductance were chosen based on performance sensitivity plots to key transistor model parameters such as transit time ($\mathrm{T_f}$), base resistance ($\mathrm{R_b}$), base-collector junction capacitance (C_{jc}), and emitter resistance ($\mathrm{R_e}$). Fig. 14 illustrates divider peak performance sensitivity to variation in these transistor model parameters. The optimal load resistance and inductance were re-extracted for high and low values of

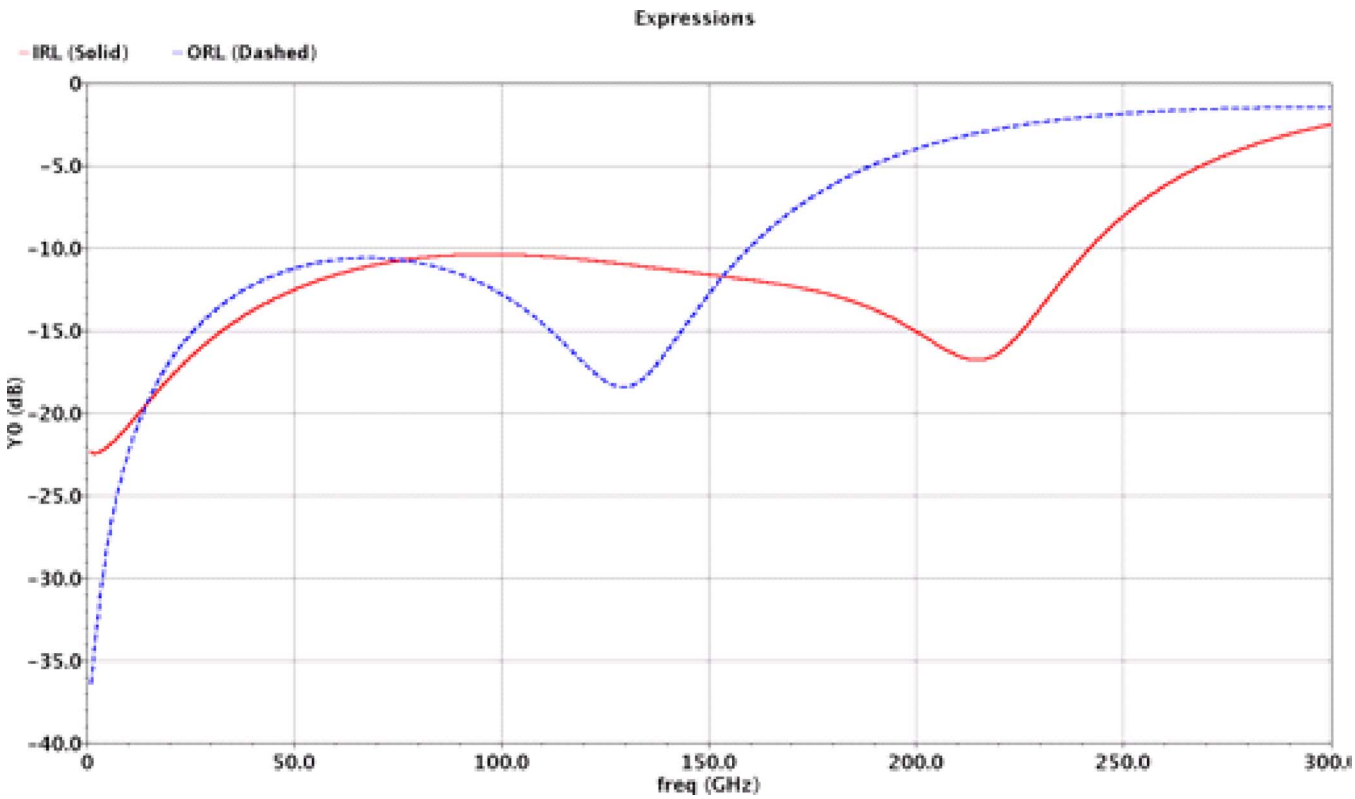

Fig. 10. Simulated input return loss (IRL)/output return loss (ORL).

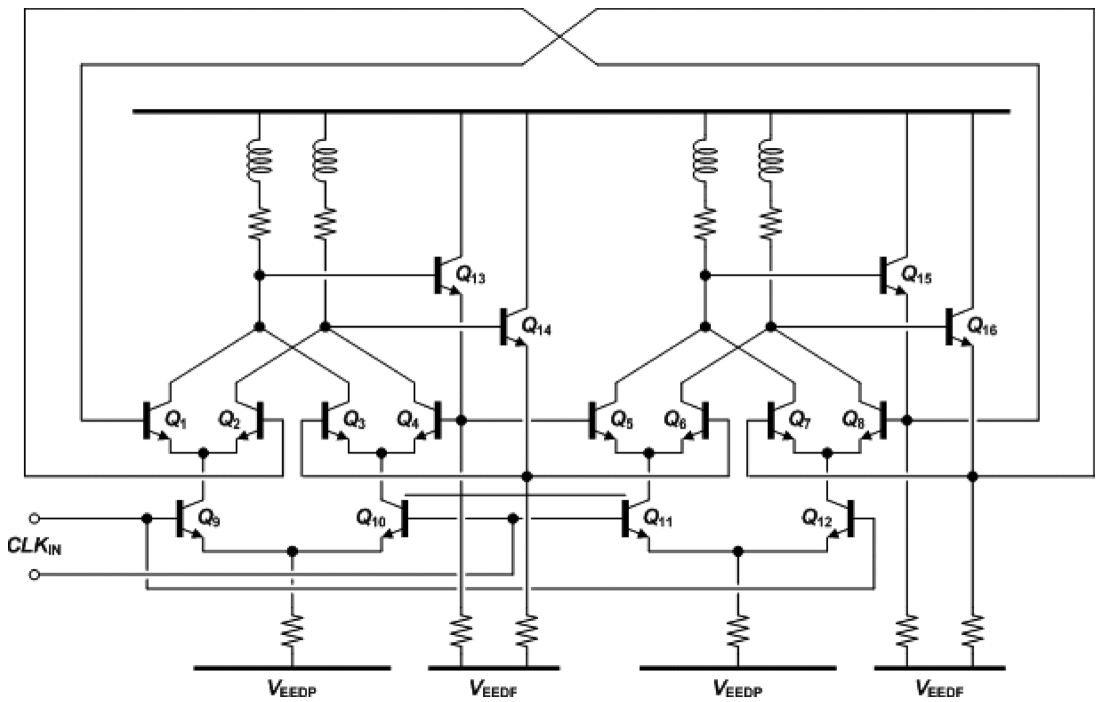

Fig. 11. Master–slave flip-flop circuit diagram.

each parameter by generating a new divider performance contour plot and finding the apex. T_f and R_b were the most sensitive parameters in the projected device models.

Fig. 15 represents an example of how the optimal load resistance and inductance vary for each transistor model parameter change. By picking wide variations in the key transistor model parameters and searching for the optimal load combinations, a trade space could be generated for systematically choosing divider variants to cover a range of HBT device and process variation to maximize the probability of obtaining an optimal

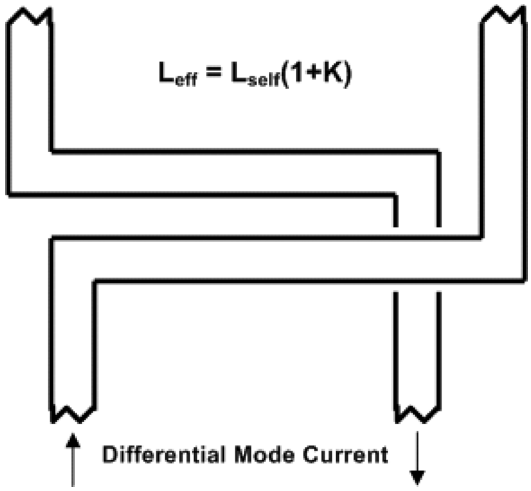

Fig. 12. Divider inductive peaking structure.

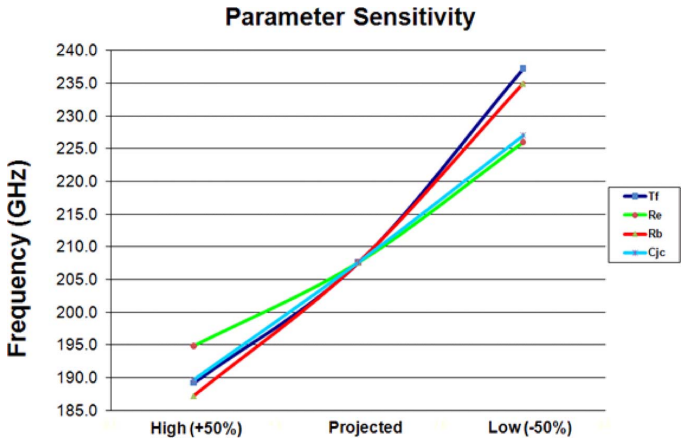

Fig. 14. Divider performance sensitivity to transistor model parameter variation.

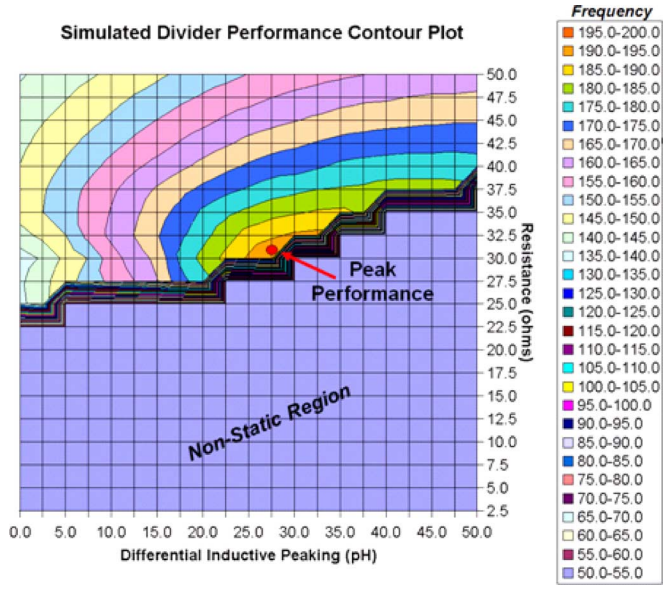

Fig. 13. Example simulated divider performance contour plot.

matched resistance/inductance load for a given HBT layout and epitaxial profile.

It was important to construct a compact divider layout to reduce parasitic capacitance and inductance which ultimately slow down the divider. The frequency divider core layout was symmetrically laid out across the horizontal axis of the die, measuring 50 μm $\times$170 μm. The transistors in the latches were oriented to minimize the critical feedback path of the master–slave latches as well as other less critical signal paths. Because of the non-conductive InP substrate, a front-side ground plane was placed selectively over the divider to minimize parasitic inductances which could have caused circuit instabilities.

C. Output Gain Buffers

The output gain buffers provide capacitive load isolation for the frequency divider core. The output gain buffer is a two-stage differential pair (Fig. 16) which runs at approximately half the current density of the master–slave latches. The pre-amplifier stage, which includes inductive peaking, isolates the divider from the final output buffer which provides the impedance transformation to 50 Ω. A broadband match similar to the front-end, using a micro-strip based inductor, is applied to the output buffer but only needs to be optimized to one half the operating range of the front-end divider input. Only one of the outputs is brought out to the bond pad. The complementary side is terminated on-chip. Better than 10 dB return loss was achieved in simulation for this interface (Fig. 10).

IV. Test and Measurement

Divider testing was performed at room temperature on a wafer probe station using a series of sources to span the full bandwidth of the divider. Nominal dual supply voltages of -6 V and -2.8 V were used for all divider tests and no bias tuning or optimization was required.

Both automated and manual wafer testing was utilized to search for the fastest divider. Automated part screening was generally done at lower fixed frequencies (such as 40 GHz or 110 GHz) with a modest fixed input RF power level (0 dBm) to establish yield patterns across the wafer which were later used during manual testing to quickly identify functional candidates for more detailed characterization of maximum operating frequency and input sensitivity. Functional part performance was defined as being able to correctly divide the input frequency by two with an output tone which was both dominant and close to the design intended power level, without the presence of spurious tones caused by bit errors. A common failure mechanism for divide-by-two's operating near maximum operating frequency manifests itself as spectral energy at the divide-by-four frequency, which is caused by occasional bit errors due to a lack of sufficient setup time in the flip-flop to make decisions in the presence of noise.

Numerous test setups were needed to cover the full bandwidth of the divider which resulted in many hours of setup changes and careful data collection. Fig. 17 provides a general block diagram of the RF test setup used for divider performance characterization. Low frequency testing down to 5 GHz was done

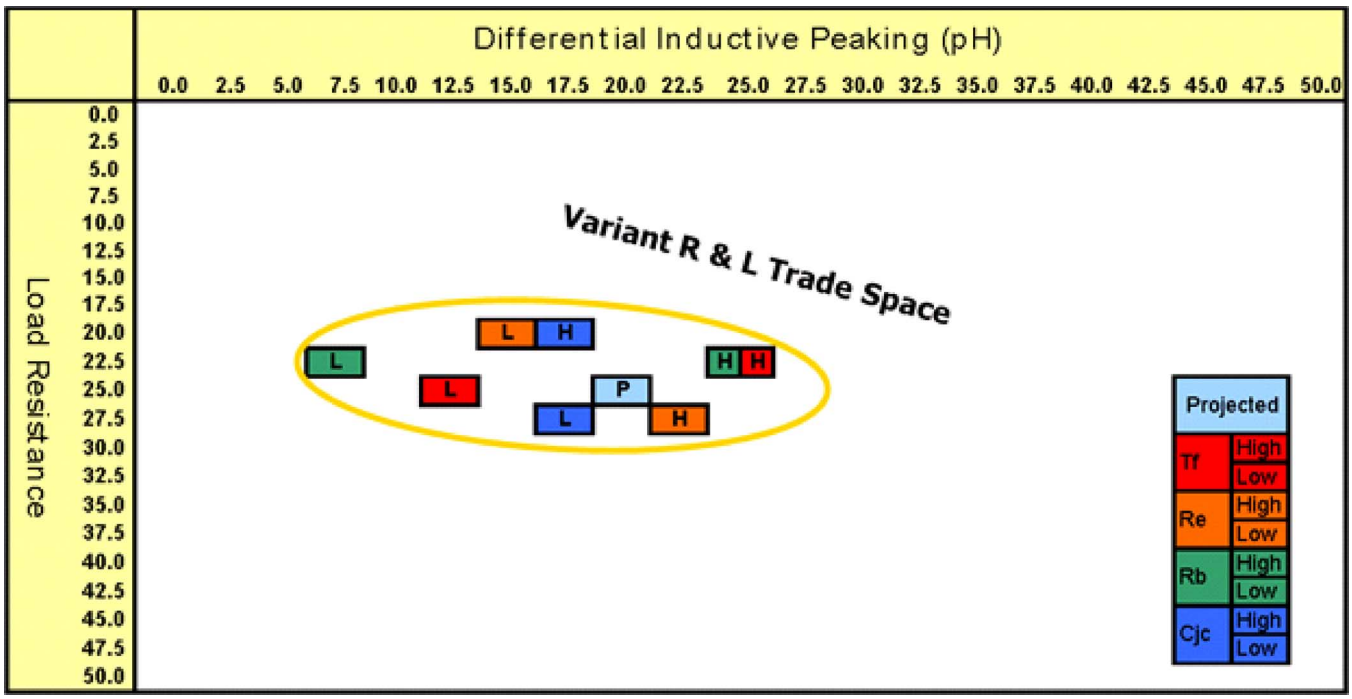

Fig. 15. Optimum R and L load sensitivity to transistor model parameter variation.

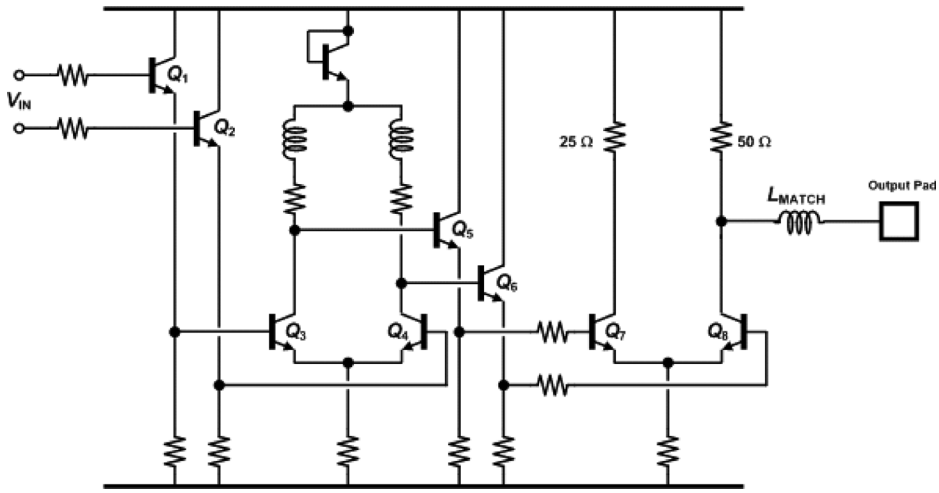

Fig. 16. Output buffer circuit diagram.

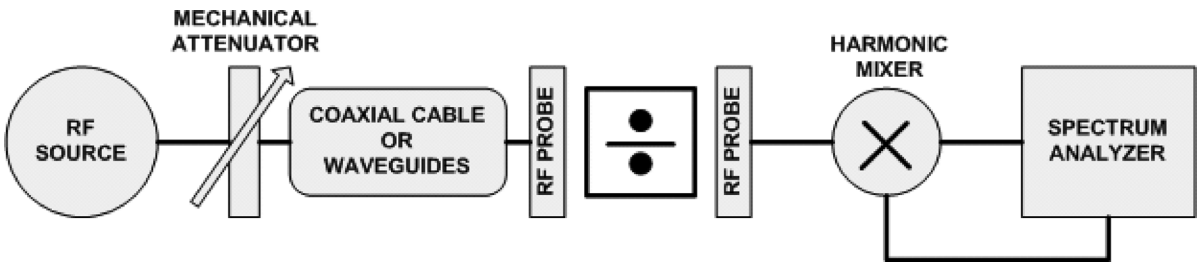

Fig. 17. RF test setup diagram.

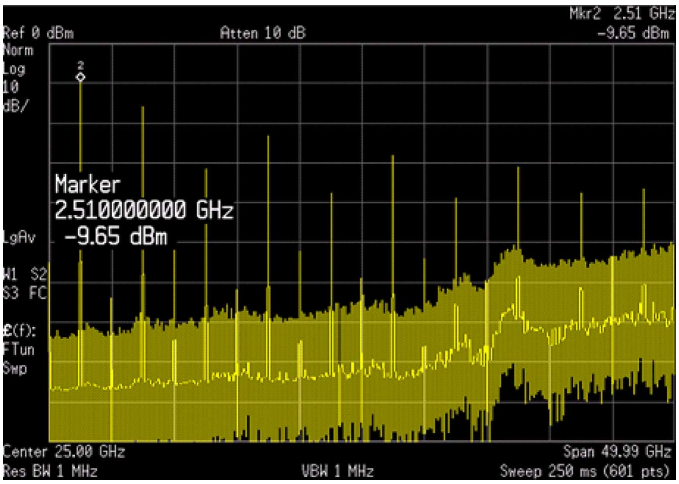

Fig. 18. Measured 5 GHz divider output spectrum of 200.6 GHz divider.

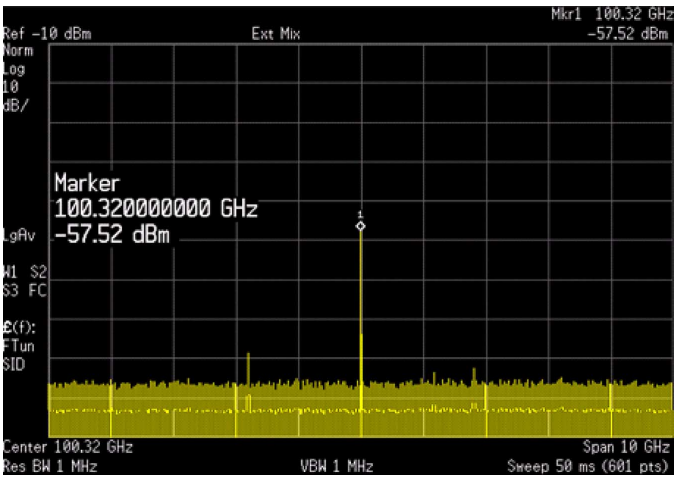

Fig. 19. Measured 200.6 GHz divider output spectrum. Output W-band harmonic mixer conversion loss is 42 dB at 100 GHz.

with a conventional Agilent 50 GHz CW source. Testing beyond 50 GHz in the V, W, D, and G-bands was performed with backward wave oscillators (BWO) from ELVA-1 or a combination of Agilent lower frequency sources, in-house amplifiers, and mixers from Virginia Diodes, Inc. depending on the band needed. Table I provides a more detailed summary of the RF source test setup. An Agilent E4448A 50 GHz spectrum analyzer was used to view the divider output. V-band or W-band harmonic mixer modules were needed on the divider output when testing above 100 GHz and 150 GHz RF inputs, respectively. Figs. 18 and 19 illustrate 5 GHz and 200.6 GHz measured operation. Note that Fig. 19 includes the conversion loss (42 dB) of the W-band harmonic mixer since it could not be calibrated out of the spectrum analyzer display. In addition we verified that over G-band operation the divider did not have any spurious divide-by-four tones, which would have constituted part failure at a given input frequency.

The divider measured versus simulated input sensitivity plot is presented in Fig. 20. A variable mechanical attenuator was used to find the minimum input power. Input power calibration was performed up to the RF probe inputs and do not include

TABLE I
RF SOURCE TEST SETUP SUMMARY

Frequency Range (GHz)	RF Source Test Setup Description
<50	Agilent 50GHz frequency synthesizer connected to RF probe with coaxial V-cable. An Agilent power meter was used for calibration.
50-75	Agilent 50GHz frequency synthesizer with Agilent V band MMIC module which outputs WR-15. WR-15 waveguides are used up to a WR-15 interface wafer probe. An Agilent V band power meter was used for calibration.
75G-110	ELVA-1 W-band BWO outputs WR-10 and connects to a variable mechanical attenuator. The attenuator outputs WR-10.WR-10 is used up to the probe which is also WR-10. An Agilent W band power meter was used for calibration.
110-130	Agilent 50GHz frequency synthesizer with a V band MMIC module outputs WR-15 to a RF amplifier. Two different amplifiers had to be used; they each cover 105-116 GHz and 116-130 GHz. The amplifier output drives a Virginia Diodes X2 multiplier which outputs WR-8. Due to lack of WR-8 waveguides we used WR-10 instead. There is a waveguide mismatch at the output of the frequency doubler. A WR-10 variable attenuator is used to vary the input power and the probe interface is also WR-10. An Agilent W band power meter was used for calibration.
140-150	Agilent 50GHz frequency synthesizer with a W band MMIC module outputs WR-10 to a RF amplifier that is WR-12 at both input and output (no waveguide transition was used). The amplifier output drives a Virginia Diodes X2 multiplier with a WR-12 input and WR-6 output. Due to the high loss of WR-5 and WR-6 waveguids we used WR-10 instead and operate it out of band. There is a waveguide mismatch between the WR-6 at the output of the doubler with a WR-5 to WR-10 waveguide transition. After a length of WR-10 there is another WR-10 to WR-5 transition to a WR-5 interface wafer probe. An ELVA-1 D band power meter was used for calibration.
154-220	The ELVA-1 G-band BWO goes as low as 154 GHz. The BWO has been custom configured to output on WR-10 size waveguide operating in the TE_{20} mode. WR-10 to WR-5 transitions join the BWO with a WR-5 variable mechanical waveguide attenuator and then a segment of WR-10. One more WR-10 to WR-5 transition connects the WR-10 to a WR-5 interface wafer probe. An ELVA-1 G band power meter was used for calibration.

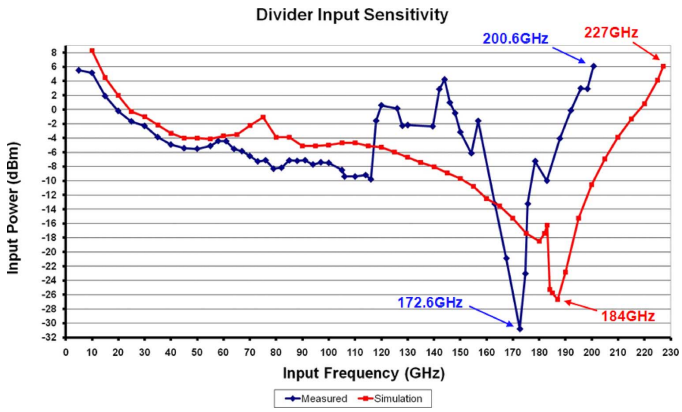

Fig. 20. Measured versus simulated divider input sensitivity plot.

the RF probe losses. The simulated input sensitivity curve consisted of using an extrapolated $\sim$600 GHz f_T transistor model, lumped-element transmission line parasitics, and the corresponding latch load values of 30 Ω and 22.5 pH. The simulated input sensitivity is in good agreement with the observed measured data.

On-wafer functional yield was also measured over a large population of parts (over 2000) using the automated RF test setup to screen dividers at a fixed input frequency of 110 GHz.

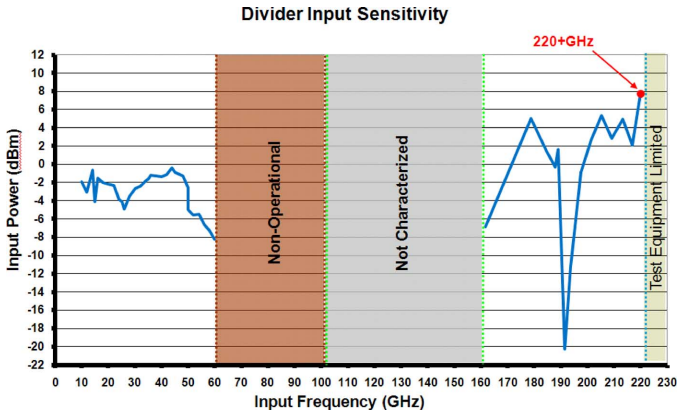

Fig. 21. Measured 220 GHz divider input sensitivity plot.

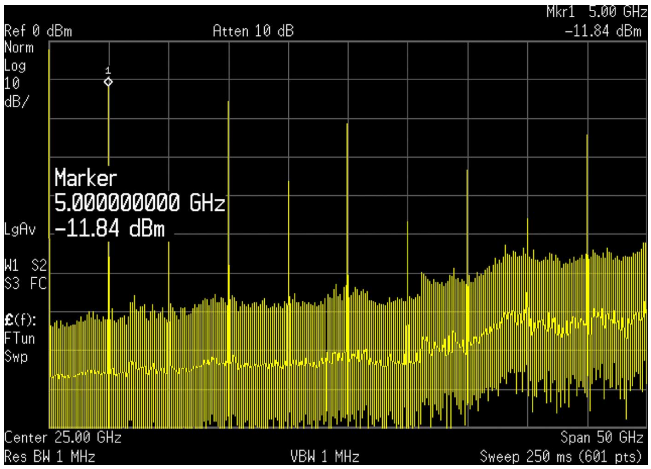

Fig. 22. Measured 10 GHz divider output spectrum of 220 GHz divider.

Dividers were considered functional when the output power at 55 GHz was within 10 dB of the expected power. Using this criterion the functional RF yield at 110 GHz was greater than 85%. It is interesting to note that in addition to the 200.6 GHz static frequency divider other divider variants were found that worked beyond 220 GHz (the limit of our test setup) but could not correctly divide-by-two in the 60 GHz–100 GHz band. These non-static 220 GHz+ dividers can be useful for certain applications but were beyond the scope of this work and as a result were not fully characterized. Fig. 21 presents the characterized and untested regions of the 220 GHz+ divider. Figs. 22 and 23 show spectrum plots of 10 GHz and 220 GHz measured operation, respectively.

V. Conclusion

We have reported a 200.6 GHz static frequency divider demonstration circuit fabricated in Northrop Grumman Corporation's advanced 0.25 μm InP DHBT process with four levels of metal interconnects. The divide-by-two core was implemented using a master–slave flip-flop with inverted feedback configuration with 0.25×3 μm^2 devices biased to

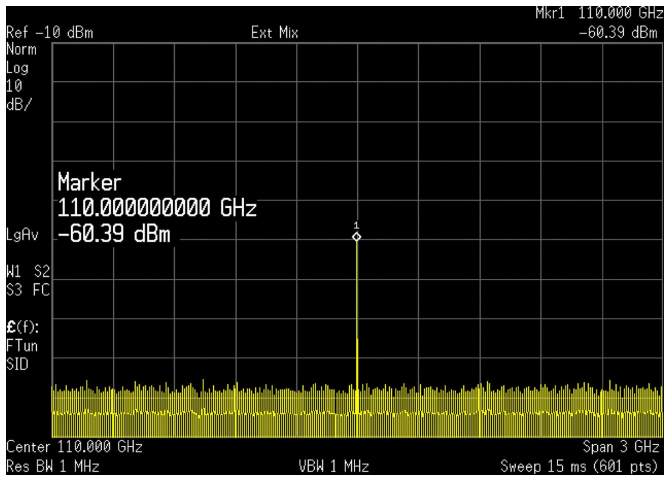

Fig. 23. Measured 220 GHz divider output spectrum. Output W-band harmonic mixer conversion loss is 46 dB at 110 GHz.

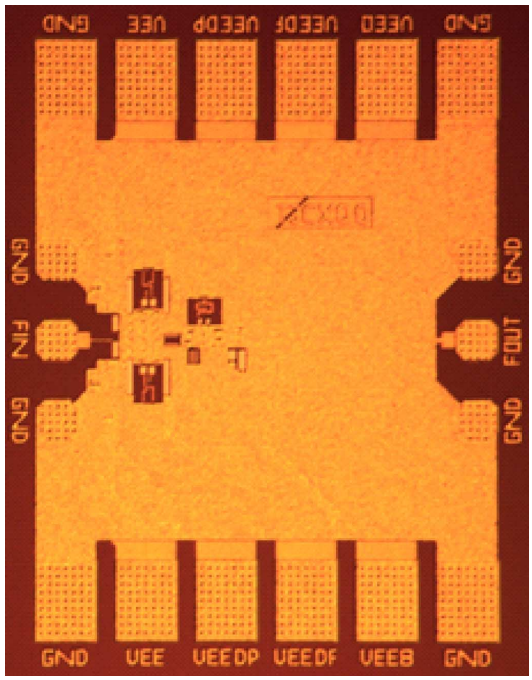

Fig. 24. Divider die photo (700 μm $\times$850 μm).

$\sim$14 mA/μm^2. The divider core flip-flop power dissipation was 228 mW. The overall die size was 700 μm $\times$ 850 μm (Fig. 24).

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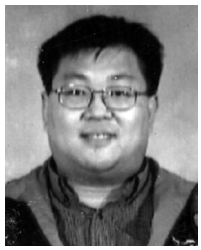

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