Multilevel Converters Criticism and a New Method to Improve High Power Applications: Restructured Controlled Transformer

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***Abstract*—Connecting power electronic devices to high voltage or high current grids has oriented relevant researches to a new challenge so called high power applications. To provide appropriate conditions to this aim, some new problems have been emerged. Multilevel power converter has been a proposed solution to increase output voltage level in the recent decades. However they really have some problems which are critically evaluated in this paper. A new solution to joint a power electronic device directly to a high voltage without any harmful effect is proposed as a high power application in the paper.**

Keywords-CSCT; High power application; Multilevel converters; EMI; Stray inductance

I. INTRODUCTION

Power electronics are finding increasing market space in industrial applications due to their imminent advantages in adjustable speed motor drives (ASD), unity power factor rectifications (PFC), active power filtering (APF), static var compensation (STATCOM), as well as unified power flow control (UPFC). Presently, most of their applications are in the low to medium power range from 5 kilowatts (kW) to 25OkW at the low voltage line of 208-480 volts (V), since high speed semiconductors such as insulated gate bipolar transistor (IGBT), MCT, and the like are readily available for these power and voltage levels. It is still a challenge to connect basic power converters, built from these types of semiconductor switches, directly to the medium-voltage grids (e.g., 2.3, 3.3, 4.16, 6.9kV and the like).

Solutions that allow connection to high power grids, such as silicon-carbide (SIC) switches, are still unproven and will take some time before introduction into commercial applications. Instead, research and development has focused on multilevel converters, which have emerged as a new breed of power converter options for high power applications.

Currently, the diode-clamped multilevel converter and cascaded H-bridge are the two most frequently used multilevel converter topologies. The diode-clamped multilevel converter, also called the neutral point clamped (NPC) converter, prevailed in the 1980's and found its applications in power factor correction, reactive power compensation, adjustable speed motor drives, and unified power flow control. However, only a limited number of levels are achievable, due to the unbalanced voltage issues in the capacitors and also due to voltage clamping requirements, circuit layout, stray inductances, electromagnetic interferences (EMI) and packaging constraints.

The cascaded H-bridge has drawn considerable interest since the mid-1990s, and has been used for ASD and reactive power compensation. The modular structure provides advantages in power scalability and maintenance and fault tolerance can be achieved by bypassing the fault modules. Unfortunately, this technology requires a large number of single- phase modules accompanied by a transformer with a large number of isolated secondary windings, resulting in high manufacturing costs. Moreover, due to its single-phase nature, each converter module processes pulsating power, resulting in a high energy storage requirement, especially in low speed, constant torque applications.

Thus, it is desirable to provide low cost converters suitable for high power applications.

The fundamental concept of high power application is to engage a device with a low or medium current but a high voltage and on the contrary with a medium voltage but a high current. These two concepts introduce devices to be connected to high potential grids as high power applications.

To connect a power electronic device to a high voltage, series switches are employed to share the voltage. However adding supplementary circuits to the switches is mandatory in order to distribute the voltage as equal including great resistors and capacitors. Moreover parallel branches of serried switches are required to pass high currents. Unfortunately these series and parallel switches can only increase the output voltage and current up to a limited level. Hence transformers are applied to augment the output voltage. However this leads to new problems which will be investigated in this paper.

II. CASCADED MULTILEVEL CONVERTERS

Fig.1 shows a schematic of a single-phase cascade converter in which two cells of traditional two-level power converters with separated DC sources are series connected [2, 3].

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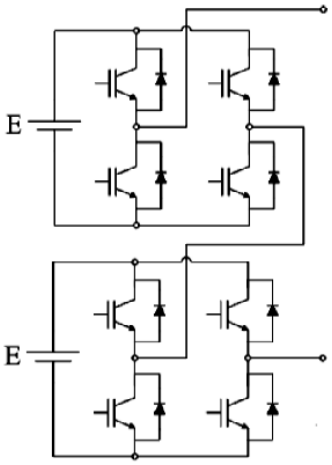

Fig.1. Single phase Cascade multilevel convener

The output waveform is synthesized by adding of each converter output voltage. Assuming the DC bus voltage of each converter is E. Based on switch combinations, five output voltage levels can be synthesized (0, ±E, ±2E).

In traditional cascade converter, the dc bus voltage of each module has the same value, and switching frequency and voltage blocking capability of all switches are the same [4].

Obviously by using proper control method applied to this topology, the stepped output waveform can be approximated to a sinusoidal waveform. Here, many algorithms can be employed, such as optimized stepped waveform method, Sub-harmonic elimination PWM method, etc. [5, 6].

In general, the output voltage of a given multilevel converter can be calculated [7] from:

$$V_o = (S - \frac{n-1}{2}).E \qquad (1)$$

Where Vo is the output of the multilevel converter, n is the number of the output levels; S is the switching state that ranges from 0 to (n-1). E is the minimum voltage level the multilevel converter can produce. For example, when S= 0, 1, 2, 3, 4, then from (1) five output levels can be synthesized respectively.

III. DIODE CLAMPED MULTILEVEL CONVERTERS

At Fig. 2, the scheme of a diode clamped multilevel inverter is shown. On the DC-side of the inverter, n different partial voltages are defined by n sources $U_1,...,U_n$. One inverter half-leg is realized with n elements connected in series, $T_1, T_2,..., T_n$, which have each their own anti parallel diode $D_1, D_2,..., D_n$. For the lower half-leg, the notation with <<'>> is used. With such an inverter scheme, the leg voltage which is defined between the output point and the negative bar of the DC link, can take N_b different values [8], according to (2).

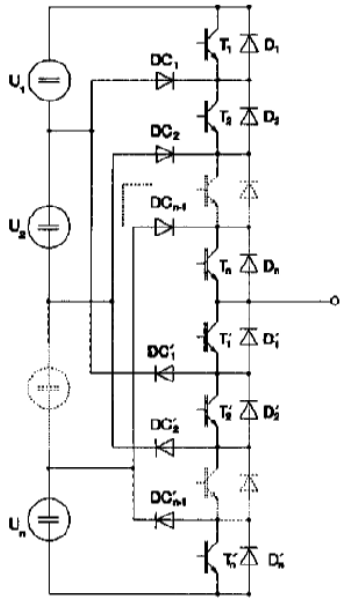

Fig. 2.General scheme of diode clamped multilevel converter (neural point clamp).

$$N_b = n + 1 \qquad (2)$$

This N_b-number defines the usual number of possible levels. The number (n) of series connected elements per half leg, which corresponds also to the number of partial-voltages at the DC-side, can be odd or even. With such an inverter leg, one-phase or three-phase inverters can be realized. The line-to-line voltage of a bridge connection realized with the described inverter leg can take a number of N_p different values, where

$$N_p = 2n + 1 \qquad (3)$$

IV. CAPACITOR CLAMPED MULTILEVEL CONVERTERS

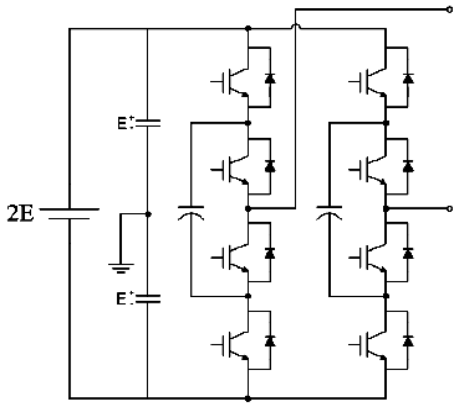

Fig. 3.Single-phase flying capacitor bi-directional converter.

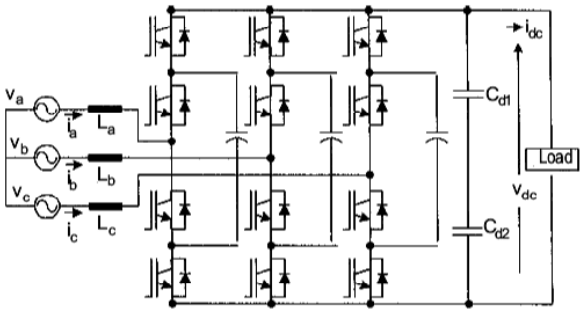

Fig. 4. Three-phase three level flying capacitor bi-directional converter.

Fig.3 shows a scheme of a single phase Capacitor clamped multilevel converter. Assuming the DC bus voltage of the converter is 2E, it can be easily found that there are five levels in the output waveform, according to (1), obtains:

$$V_o = (S-2).E \tag{4}$$

Where E is the minimum voltage level, S=0, 1, 2, 3, 4. For S select 0, 1, 2, 3, 4, five different values of the output voltage can be achieved, i.e. (0, ±E, ±2E) accordingly. Approximate sinusoidal output waveform can be achieved by applying proper control methods [5].

Fig. 4 and Fig. 5 represent three phase three and five level converters respectively. It is clear from these figures that more capacitors are engaged to have more output voltage levels. Each capacitor should have a particular fixed voltage to operate appropriately.

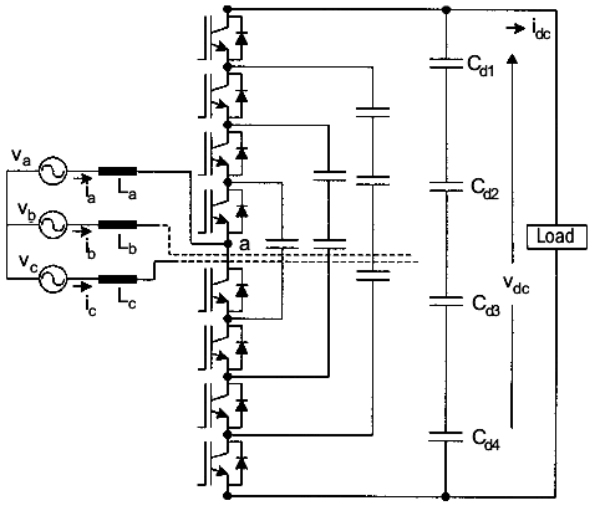

Fig. 5. Three-phase five level flying capacitor bi-directional converter.

The main problems of these converters are pertaining to unbalanced voltage of dc link and flying capacitors, stray inductances especially in high frequencies of control, much number of switches, diodes and capacitors, content of harmonics in the output voltage and electromagnetic interference (EMI).

In the case of diode clamped multilevel converters, below problems can be briefly classified in addition to mentioned problems [9]:

a) Indirect clamping of the Inner devices:

In a normal two level inverter leg, each switch is directly clamped to the dc link capacitor by the opposite freewheeling diode. And no static over-voltage will possibly appear across the switch while transient voltage spike resulted from energy release of the stray inductance at the moment of commutation can be happened across the switch. Switches in the diode clamping inverter, however, are actually not directly clamped to the dc link capacitors, except for the lateral two switches ($T_1, T_n^{'}$ in Fig. 2). Depending on the stray inductances of the structure, any indirectly clamped switch may tolerate more than the nominal blocking voltage, which is $V_{dc}/(n-1)$ for an n-level inverter, during its OFF state.

b) Turn-on snubbing for the inner dc rails:

Among the n DC-rails of an n-level diode clamping inverter, each of the inner (n-2) rails has to carry bidirectional controlled current. As in the case of matrix converter, a bidirectional current controlled rail prevents the use of polarized turn-on snubber. Nonpolarized snubber is known to be especially inefficient [10].

c) Multiple blocking voltages of the clamping diodes:

Even though each main switch is supposed to block the nominal blocking voltage, the blocking voltage of each clamping diode in the diode clamping inverter is dependent on its position in the structure. For a -level leg, one can find two diodes each sees blocking voltage of

$$V_{diode} = \frac{n-1-k}{n-1}.V_{dc} \tag{5}$$

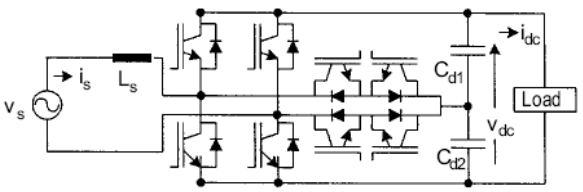

Fig. 6. Modified single phase diode clamped converter with parallel switches to the clamping diodes.

V. CRITICAL EVALUATION OF MULTILEVEL CONVERTERS

where n is the number of levels, k goes from 1 to n-2 and V_{dc} is the total dc link voltage. The indirect clamping problem comes inherently with the diode clamping structure of the circuit. Unless an active switch be put in parallel with each clamping diode (which achieves direct clamping) (see Fig. 6), the problem may not be removed however the problem will be mitigated when stray inductance is reduced, or when an effective auxiliary clamping is installed. As a result of the turn-on snubbing problem, use of switching devices like GTO's or IGCT's in the diode clamping inverter is thought to be a challenging subject. dc rails polarized turn-on snubbers [11] will worsen the static over-voltage problem of the inner devices.

d) Stray inductances and capacitances

Stray inductances and capacitances in the path of current can cause a sever over voltage on some of the clamping diodes. This problem will lead designers to engage auxiliary resistors in parallel to diodes which results a surplus power loss.

Any circuit of finite size has stray inductance due to the magnetic fields created by the current carrying conductors, but techniques of minimizing these effects are well established. They include twisted-pair, bus-bar, and other flat-plane constructions in which the "go" and "return" currents are distributed and in close proximity, thereby achieving the maximum cancellation of the magnetic field and minimum inductance. The stray inductance interacts with the high rates of current in the circuit to produce voltage spikes across a power semiconductor as it switches off. Typically, an 80-mm loop of wire has an inductance of 1 μH, across which a voltage of 300 V would be induced with a di/dt of 300 A/μs.

A further effect of stray circuit inductance is to increase dissipation in the power semiconductors as the stored energy in stray inductance is discharged into them when they switch off. This loss is given by $(1/2)Li^2 f_s$, which for a circuit with 1- μH stray inductance, say, carrying 100 A and switching at 10 kHz, works out to be 50 W.

Stray inductance, therefore, causes two circuit effects. The voltage spike associated with di/dt depends on device switching speed, but the additional loss is independent of rate of change of current.

Minimizing or eliminating this form of stray circuit inductance, by wise bus-bar design can, therefore, obviate the need for snubber components, reduce the temperature rise of active silicon and facilitate the use of higher switching frequencies. It is a vitally important aspect of circuit design

The above understanding of the general impact of stray inductance on circuit performance bears the question: What is the optimum switching speed for a device? The answer appears to be, just fast enough to perform the required duty in the circuit. Faster is the switching speed, there would be more unnecessarily high voltage spikes.

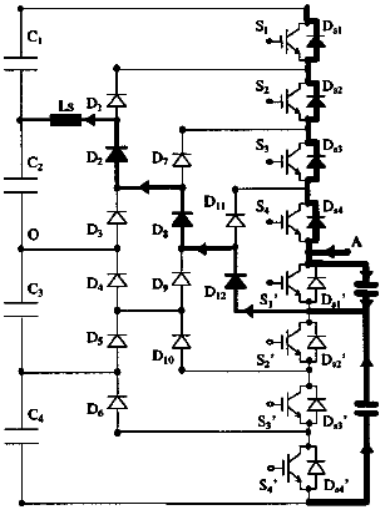

Fig. 7. Stray inductance demagnetization during the commutation process from $S_1^{'}, D_{12}, D_8$ and D_2 to D_{s1}, D_{s2}, D_{s3} and D_{s4} in the diode clamped converter.

An "ideal" device that switches off in zero time would cause infinitely large voltage spikes unless the circuit is also "ideal" and has zero stray inductance [13].

Reference [9] has proposed a new structure of diode clamping multilevel inverter to mitigate some mentioned problems however problem d is still not solved without auxiliary resistors. Here this proposed structure and the problem are presented:

Indirect clamping will possibly result in unequal voltage distribution among the blocking devices, due mainly to the stray inductances in the structure.

In the following text, the commutation process from $S_1^{'}, D_{12}^{'}, D_8^{'}, D_2$ to $D_{s4}, D_{s3}^{'}, D_{s2}^{'}, D_{s1}$ will be considered. As $S_1^{'}$ is indirectly clamped, $S_1^{'}, D_{11}$ and D_7 will have to block more than the nominal voltage during the OFF state. Prior to commutation, S_2, S_3 and S_4 are ON. Upon the releasing of the turn-off signal for $S_1^{'}$, the stray capacitance of $S_1^{'}$ will first be charged. Until the voltage across the stray capacitance of $S_1^{'}$ reaches $V_{dc}/4$, freewheeling diodes D_{s1}, D_{s2}, D_{s3} and D_{s4} will conduct, leading to demagnetization of the stray inductance (L_s) in the clamping path, as shown in Fig. 7. The trapped energy in L_s will be absorbed by the stray capacitance of $S_1^{'}$ together with the stray capacitances of $S_2^{'}, S_3^{'}$ and $S_4^{'}$. The stray capacitance of $S_1^{'}$ will continue be charged, whereas the stray capacitances of

S_2', S_3' and S_4' will be discharged. Such over-charging and discharging will not be recovered subsequently, as the discharging path for the stray capacitance of S_1', and the charging path for the stray capacitances of S_2', S_3' and S_4' are both blocked by D_2, D_8' and D_{12}'. Consequently, S_1' will block more than $V_{dc}/4$ voltage while S_2', S_3' and S_4' together will block less than $3V_{dc}/4$ voltage during the steady state.

Moreover, D_2, D_8' and D_{12}' together sees the difference between the blocking voltage of S_1' and $V_{dc}/4$. Meanwhile, D_{11} sees $V_{dc}/4$ plus V_{D2} and V_{D8}, D_7' sees $V_{dc}/4$ plus V_{D2}, while D_1 sees $V_{dc}/4$.

Due to the fact that the stray capacitance of the neighboring outer switch experiences one more discharging than the inner switch, among the blocking devices, the outer switch will always block less voltage while the inner device will always block more voltage. The center device will always be exposed to the highest voltage stress.

With refined bus-bar designing technique, and in particular, appropriate positioning of an auxiliary clamping, the problem will be mitigated. This configuration is shown in Fig. 8.

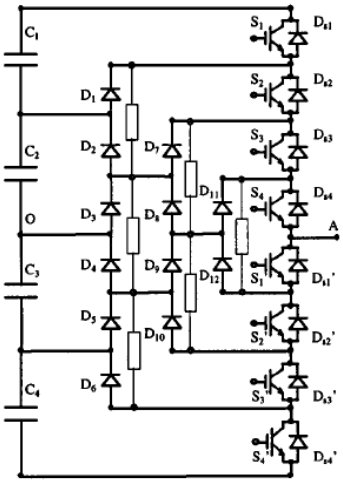

Fig. 8. An auxiliary clamping network configuration for the diode clamping inverter.

e) Electromagnetic interference (EMI)

A major advantage of the progress in power semiconductor technology is the possibility to increase power density for energy conversion devices by reducing space for energy storage and cooling. Especially in the power range up to 100kW converter size is an important issue. Manufacturers minimize the size by integrating power components, heat sink and control electronics. Thereby severe problems arise due to electromagnetic interaction between close components, which often lead to malfunction and EMC (Electromagnetic Compatibility) problems. Especially EMC filters being very sensitive to electric or magnetic fields, cause extra cost for screening or for additional space [12].

Reference [12] has outlined an electromagnetic interference simulation for principal elements using in multilevel converters such as capacitor, inductor, mutual inductors with an inner core and harmonic filters. Moreover, reference [13] has illustrated and simulated this phenomenon for power semiconductors and iron cores of transformers under high frequency and variations of voltages and currents in multilevel converters.

It can be derived from these references that electromagnetic interference would be more critical as the frequency of closing the switches becomes greater. Since these converters will not be able to be connected to a high voltage without any transformer as a high power application, increasing the frequency of switching in order to decline harmonic components should be confined so that the produced EMI in the transformer and other mentioned devices would be ambient. Hence a trade-off should be anticipated.

f) Unbalanced capacitors

There are two considerations in this problem. First one is unbalanced capacitors in dc link. Application of traditional modulation techniques to the diode or capacitor clamped converter causes a low-frequency oscillation of the dc-link capacitor voltages. This, in turn, increases the voltage stress on the devices and generates low-order harmonics in the output voltage [14].

Second one is to fix the voltage of flying capacitors in capacitor clamped converters. Since the object of applying capacitors is to have an special stepped dc voltage in the output in an operating mode of switches, the voltage of each flying capacitor should be held fixed on its nominal value however the voltage of these capacitors would be under variations due to operating semiconductors leading to change the path of current. Keeping these voltages fixed calls for intricate calculations and designs and probably expensive instruments.

VI. CSCT AS A NEW HIGH POWER APPLICATION

Controlled Shunt Compensator of Transformer type (CSCT) is a high power application device which is controlled by thyristor and can be connected to a high voltage such as 500 KV directly.

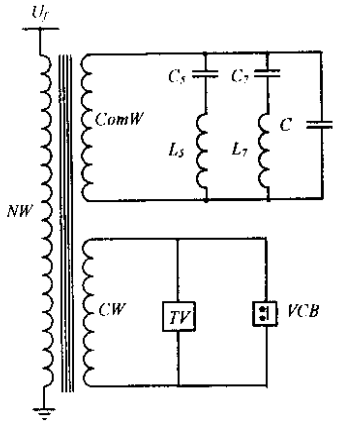

Fig. 9. General scheme of a CSCT: TV-thyristors valve, VCB-vacuum circuit breaker, C5-L5 and C7-L7 filters of fifth and seventh harmonics, C- additional capacitor bank.

A general scheme of this compensator is presented in Fig. 9. This configuration is a transformer with three windings. NW is network winding which is connected to the network and is the main winding of the compensator. CW is the second winding to which a thyristor valve and a parallel voltage circuit breaker are connected and is called CW briefly. The third winding is compensating winding which is indicated by ComW in Fig. 9. Two highest harmonic filters and a capacitor bank are connected to this winding. It is important to note that CSCT is a three phase compensator. The connection of NWs of three phases is star and the neutral is grounded. Control windings' connection is as same as network windings of three phases. However compensating windings are delta in connection together in order to eliminate third harmonic of the current.

VCB in the Fig. 9 is a vacuum circuit breaker which can switch on or off CW while repairing or changing the thyristors without disconnecting CSCT from the network.

Fig. 10 represents one phase of the transformer with mentioned three windings. The winding close to the main core is CW, the outer winding is NW and interlaid winding is ComW.

Now let's consider circumstance of operation of this structure. When CW is open circuit by the thyristor, all the magnetic flux produced by network winding connecting to network passes through the magnetic core of the transformer. Since permeability of the magnetic core is about 3000 times greater than the permeability of the vacuum, the magnetic flux passing through the air gap encompassing three windings is negligible in comparison with the core. So the effective cross-section of magnetic flux path is the area of the core in this mode. As a result, when the thyristor is opened, equivalent reluctance of the transformer is small. So the inductance of CSCT is great. Thus a minimum current, magnetizing current, will pass through network winding. Since all of the windings include the magnetic flux in the core, even if there was not capacitor bank, the induced current in the network winding from ComW is capacitive because of the capacitors of highest harmonic filters connected to ComW. The value of this capacitive current can be increased to an arbitrary value by adding a capacitor with a corresponding value to the ComW circuit.

As a result, in open circuit mode of the thyristor, value of the capacitor determines the maximum capacitive current of the compensator; however value of the capacitors of the harmonic filters that if there was not any capacitor bank.

Now imagine the short circuit condition of the thyristor and consequently the control winding. In such a condition, the magnetic core emplaces a barricade preventing the flux to pass. Hence the magnetic flux produced by network winding is forced to flow through construction elements such as covers and walls of tank or other metallic parts of the transformer and this phenomenon causes a significant power loss in the transformer approximately equal to copper losses in the coils. In order to avoid occurring this problem, two magnetic shunts are installed above and bottom of all of the windings. The inner diameter of these disks is equal to the inner diameter of CW and correspondingly the outer diameter of them is equal to outer diameter of NW. Six magnetic shunts are used for three phases, two of them for each phase. Magnetic shunts collect the dissipated flux and send it to the yokes tightened to the main core. After using these magnetic shunts, the mentioned additional loss will be reduced up to 10% of the copper losses. In this situation much of the magnetic flux gets out of magnetic shunts to pass through the air gap encompassing all the windings and the remained flux flows in lateral yokes after passing magnetic shunts. In this case permeability of the magnetic flux path is decreased up to the permeability of the vacuum.

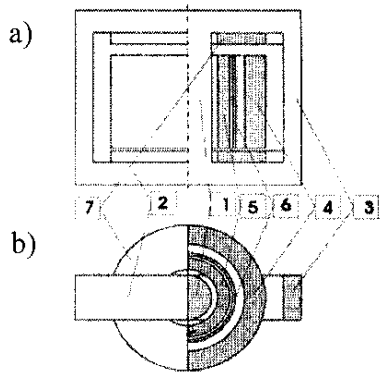

Fig. 10. Mono phase diagram of CSCT: a- view form side; b- view form above: 1- a main core, 2- yokes, 3- lateral yokes, 4- NW, 5- CW, 6- ComW, 7- magnetic shunts.

Moreover the cross-section of the magnetic flux path is significantly greater than the short circuit of the thyristor mode. Consequently the reluctance of the magnetic flux path is about 300 times greater than the previous. Hence the equivalent inductance of CSCT will be minimal. In this mode, the maximum inductive current will pass through network windings and accordingly consumption of reactive power will be maximal so called the rated power of the CSCT.

Two modes of operation of CSCT were illustrated. In summarized, in the first mode the thyristor was opened and a reactive power was injected to the network. The other mode was short circuit of the thyristor. In this mode the nominal reactive power was consumed by CSCT from the network. Since in both modes the current of NW has capacitive or inductive characteristic, it has a ±90º in relation to phase of the voltage.

Intermediate capacitive or inductive powers can be obtained according to intermediate firing angle of the thyristor. Firing angle of the thyristor can change in range of 90º-180º in relation to the phase of voltage.

The relation of current of NW to the rated value according to different values of firing angle of the thyristor is shown in Fig. 11. It is found from this figure that the current of NW is equal to the rated value corresponding to the firing angle of 90º. As the firing angle increases, the inductive current decreases so that it reaches to zero in a particular firing angle.

Six curves have different schemes in relation to different values of the capacitor bank. Increasing the firing angle in greater values causes the current to be capacitive.

Compensation windings with a delta connection have been designed to eliminate third harmonic.

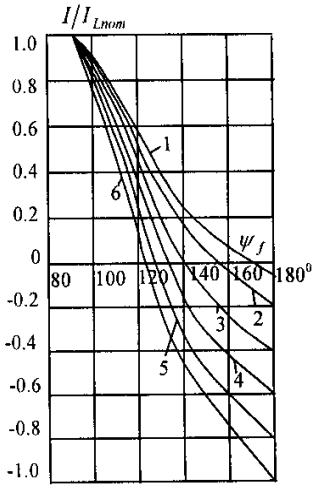

Fig. 11. The current in NW of CSCT versus the firing angle of thyristors by: C=0 (curve 1), $I_{C,nom} / I_{L,nom} = 0.2$ (curve 2), 0.4 (curve 3), 0.6 (curve 4), 0.8 (curve 5), 1 (curve 6).

In order to damp fifth and seventh harmonics of the current, two adapted filters are used. Each of them is a capacitor serried by an inductor which is in resonant in the corresponding frequency.

It is clear that these filters show a capacitive treatment in the basic frequency.

Total capacitance of filters is about 10% of the rated capacity of the compensator.

Voltage of ComW is less than the voltage of NW and current of Comw is about four times more than current of NW. Thus the content of highest harmonics in the current of NW is less than 2% of the rated current of CSCT as the simulation results prove this claim.

Now it is important to consider the characteristic parameters of CSCT as an efficient high power application.

CSCT can be connected to a high voltage directly because of its transformer aspect and having a 100% voltage in NW in condition of short circuit in CW even in ComW so that this characteristic bears it out of mind to use any protective circuit breakers.

Moreover, the thyristor is turned on and off only one time during a power frequency cycle resulting not to produce any EMI or stray inductances and capacitances especially in the transformer.

An important characteristic of this device is that there is only one thyristor block which controls the output current so the gate control circuit is very simple and convenient to install in addition to a simple and cheap cooling system in comparison with multilevel converters which require many heat sinks.

VII. CONCLUSION

Multilevel converters are classified and briefly considered using various relevant papers. The main problems of these devices as high power applications are also considered.

Stray inductances and capacitances, EMI problems, complexity of balancing the voltage of flying capacitors and the capacitors of dc link, ununified dispersed voltage on the clamping diodes, harmonic components and many other problems of multilevel converters cause to find new solutions devices to mitigate these problems.

If we refer to the reason which led to introduce multilevel converters, increasing the voltage level in the output in order to connect to a high voltage, we can present new combinations which can satisfy the idea without causing critical problems. CSCT is such a device whose main part is a transformer which can connect to a high voltage directly. In this device the transformer is not a connector between power electronic device and high voltage but also is the main element of the device. Since the thyristor imposes one winding of the transformer to be short circuit in an arbitrary duty cycle, restructuring of the iron core is done by installing additional irons to the conventional transformer.

The simulation and experimental results prove that CSCT can connect directly to a desirable voltage level having good performance as high power application, low harmonic components, low power losses, low costs, simple installation and high reliability.

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