New Transformerless Medium-Voltage STATCOM based on Half-Bridge Cascaded Converters

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***Abstract*--To achieve higher performance in a distorted and unbalanced medium-voltage large-current system, a new shunt compensator is presented based on half-bridge cascaded converters (HBCC). Then, the transformerless HBCC based STATCOM can be controlled for various purposes such as reactive power of STATCOM, simultaneous harmonic cancellation and load balancing procedure. Compared to the conventional modular multilevel converters, the HBCC based STATCOM introduces lower ratings both for active and passive elements, improving the overall efficiency of the converter. A control strategy is proposed to ensure the source-end three phase currents are sinusoidal and balanced. At the same time, the DC capacitors voltages are controlled to operate under balanced condition. One interesting application for the HBCC based STATCOM could be electric traction system. Both power circuit and the proposed control strategy are simulated with PSIM and MATLAB, confirming the pre-defined objectives.**

***Index Terms*--Cascaded converters, Half-bridge, Medium voltage, STATCOM, Unbalanced load**

I. Introduction

MODERN medium-voltage distribution systems are proliferated with non-linear loads such as single-phase AC traction systems. In addition to the harmonic penetration, these loads enforce significant unbalances to the network. Therefore, the associated problems of reactive and harmonic compensation plus load balancing are inevitable and ought to be considered simultaneously to achieve acceptable power quality level. Meanwhile, mitigation of all these power quality problems by means of a single compensator is a challenging task [1-2]. Previously, static synchronous compensators (STATCOMs) based on multi-pulse voltage source converters were proposed in [3-4], which comprise VSCs and one or more transformers with sophisticated winding connections. These transformers are used to increase the level of output voltage through complex magnetic circuit configurations. On the other hand, such circuit structures produce serious problems like high losses, saturation, non-linear operation of the core plus the effects on the control loop by the compensator, voltage impulse production, high costs and finally, the size.

Full-bridge cascaded converters (FBCCs) could be directly connected to medium voltage networks [5-6]. Unlike diode-clamped converters and capacitor-clamped converters, FBCCs introduce smaller total losses along with higher reliability. But the FBCCs do have their short comings when operating under distorted unbalance situations in a medium-voltage network compared to those of diode-clamped and capacitor-clamped converters [1-7]. In order to thrash out these limitations, a new STATCOM based on M^2LC [8-9], is proposed in this paper. As shown in Fig. 1(A), the proposed compensator has two half-bridge cascaded converters (HBCC) connected in parallel which can be used for parallel compensation of reactive power, harmonics and load balancing. The active power exchange in the internal loops of this topology could be used for load balancing, while the voltages of all DC capacitors remain balanced. The converter structure and operation is described in Section II. Section III describes control of a basic version of the proposed STATCOM. It is shown that the capacitor voltages of the half-bridge modules (HBMs) can be stabilized by proper controlling. Simulations confirm the operation of the basic form of new HBCC based STATCOM.

II. Converter Description and Operation

The proposed converter of this compensator consists of two parallel HBCCs. The both HBCC are identical and comprised of four legs with star configuration, for compensation of a three-phase four-wire load. As shown in Fig. 1(B), in an *n* level proposed converter, each leg of the HBCCs consist of *n-1* identical half-bridge modules (HBMs) and a filter inductor connected in series. All HBMs have the same semiconductor ratings as well as the same capacitance. Therefore, all HBMs are identical 2-terminal devices. Voltage regulation of the DC-link capacitors is achieved without any additional connections or energy transfer circuits to the associated HBMs. In accordance with Fig. 2(B), each HBM is capable of producing the instantaneous voltages $+V_{Cm}$ and 0 depend on its command signal. Thereupon, according to Fig. 1(B), terminal voltage of a leg in each HBCC can take the value:

$$V_{xm}=V_{xm,1}+V_{xm,2}+ \dots + V_{xm,(n-1)} \qquad (1)$$

($x = A, B, C$ or N; and $m = 1$ or 2)

According to Fig. 1, in this equation m is *1* for upper HBCC and *2* for lower HBCC. Also x correspond with phase, namely *A*, *B*, *C*; and *N* for legs connected to the neural network point.

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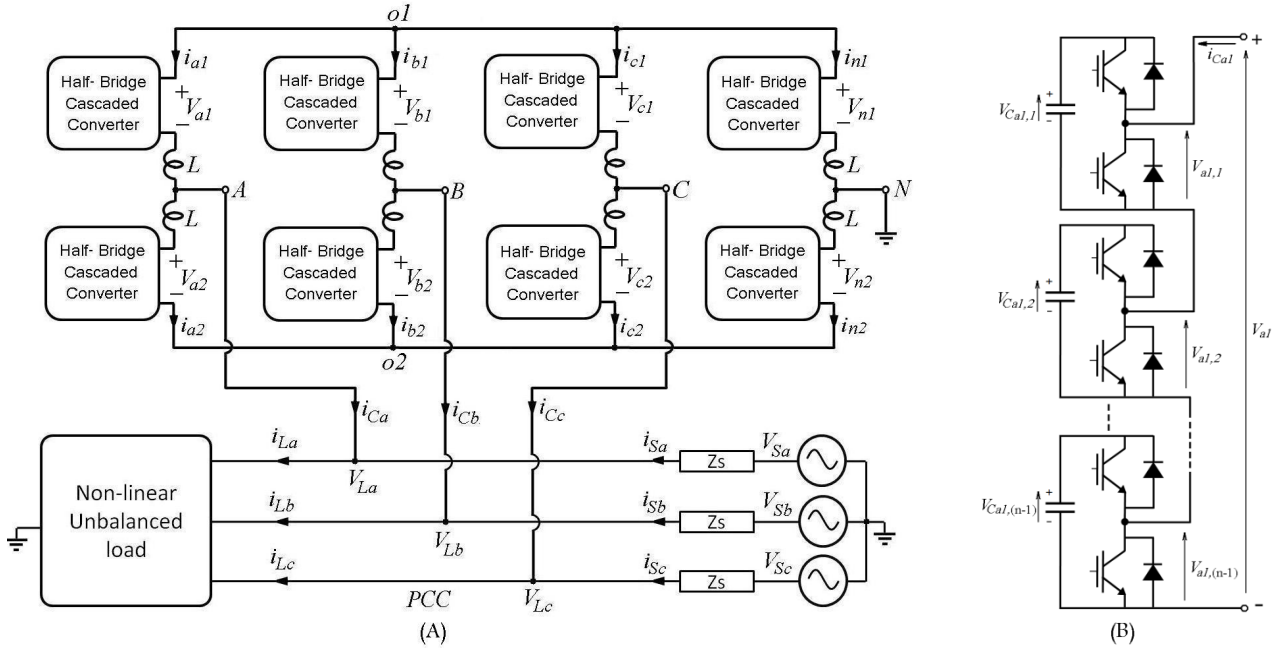

Fig.1 (A) Configuration of the new transformerless STATCOM topology, (B) Configuration of the upper HBCC of the proposed converter in phase

Minimum output voltage that a leg in each HBCC can produce is zero and maximum output voltage that a leg in each HBCC can produce is $(n-1).V_{Cm}$. Therefore output voltage of each leg is always positive while the voltage between two terminals of each HBCC can be adjusted between $+V_{DCM}$ and $-V_{DCM}$. Also the value of capacitor voltage of each HBM must be adjusted to below value:

$$V_{Cm}=\frac{V_{DCM}}{(n-1)} \qquad (2)$$

The V_{DCM} is maximum instantaneous voltage of each leg and it must be greater than of the maximum value of line voltages. Due to the fact that each HBCC provides half of the output current of the compensator, voltage across legs of upper and lower HBCCs, connected to the same phase, are constantly in complementary form. In other words the voltage between upper connection point ($o1$) and lower connection point ($o2$) equals to V_{DCM} at every instant, namely:

$$V_{x1}+V_{x2}=V_{DCM} \qquad (3)$$

As a result, irrespective of the filter inductors voltages, the voltage between upper and lower HBCCs connection points (V_{o1}-V_{o2}) is always V_{DCM} ; while the voltage between the V_{o1} and the neural network point (V_N) is $+V_{DCM}/2$ and the voltage between V_{o2} and V_N is $-V_{DCM}/2$ as shown in Fig. 2(A).

When the converter provides unbalanced current to rebalance and compensate the nonlinear unbalanced load, one output terminal of the converter produces active power while the other terminals consume active power. It tends to reduce the capacitors' voltage of HBCCs' legs that provide active power and increase the capacitors' voltage of HBCCs' legs that consume active power. It further causes a direct current (I_B) flow from the HBCCs' legs consuming active power part while providing active power to the HBCCs' legs. Since upper and lower HBCCs in each phase leg provide or consume half of the active power of corresponding phase, magnitude of direct current in the upper phase leg (I_{Bx1}) is the same as magnitude of direct current in the lower phase leg (I_{Bx2}). In other words we have $I_{Bx1} = I_{Bx2} = I_{Bx}$. Under such circumstances, total current of each HBCC is equal to:

$$\begin{bmatrix} i_{x1} \\ i_{x2} \end{bmatrix}=\begin{bmatrix} \frac{i_{Cx}}{2}-I_{Bx} \\ -\frac{i_{Cx}}{2}-I_{Bx} \end{bmatrix} \qquad (4)$$

The magnitude of balancing current (I_{Bx}) in each phase leg depends on the value of active power that will flow into or out of that phase leg. In realization of three or four legged HBCC based STATCOM, the sum of the total converter balancing currents will always be zero ($I_{BA}+I_{BB}+I_{BC}+I_{BN}=0$). Therefore, electrical energy of all HBCCs' legs remains balance. It is proved in the next part by equation (7). Because of the filter inductors in series with HBCCs' legs, the increased current fluctuation of output converter currents can be damped substantially.

One of the advantages of the proposed compensator converter is that it can balance the network current in compliance with changes in load or even the impedance and the voltage of the network. The way through which voltages of all storage capacitors can be controlled is explained as follows.

III. CONTROL

The controller of the proposed HBCC based STATCOM must perform the following major tasks:

1. *Calculate proper output currents of the converter*
2. *Calculate reference voltage of the HBCCs' legs*

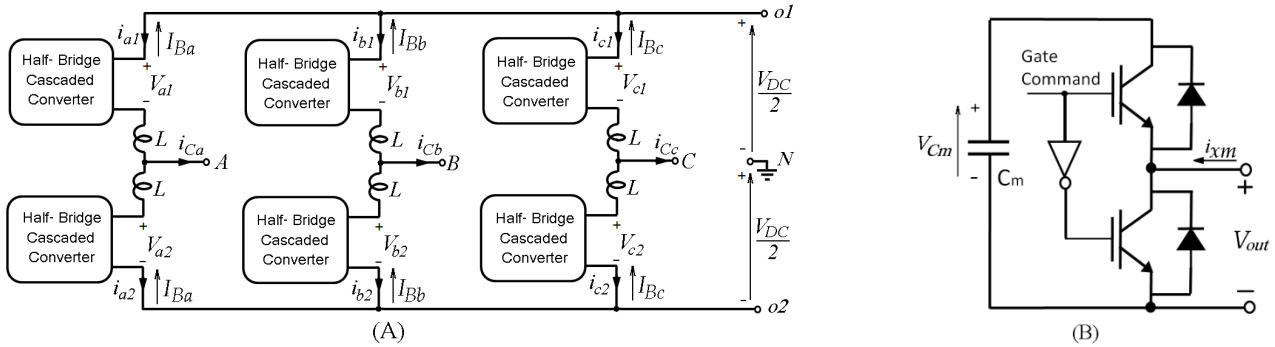

Fig. 2(A) Description of three-phase three-wire HBCC based STATCOM topology, (B) Schematic of an HB inverter and its switches command

3. Generate switching signals and also

4. DC storage capacitors voltage balancing

The control system that accomplishes the above four tasks simultaneously is demonstrated here. We utilize the general instantaneous power theory [10] to calculate the current reference signals for each phase of the compensator as described in Fig. 3. The objective of this compensation theory is to make the currents of source completely sinusoidal, balanced and in phase with the first harmonic of positive sequence of source voltage. By having the voltage of point of common coupling (PCC) and reference current of compensator, the voltage of upper and lower HBCCs in each phase can be calculated as follows:

$$\begin{bmatrix} V_{x1} \\ V_{x2} \end{bmatrix} = \begin{bmatrix} \frac{V_{DCM}}{2} - V_{Lx} - L\frac{di_{Cx}}{2dt} \\ \frac{V_{DCM}}{2} + V_{Lx} + L\frac{di_{Cx}}{2dt} \end{bmatrix} \quad (5)$$

By a good approximation we write the above equation for a single switching period as:

$$\begin{bmatrix} V_{x1} \\ V_{x2} \end{bmatrix} = \begin{bmatrix} \frac{V_{DCM}}{2} - V_{Lx} - \frac{L(i_{Cx(ref)} - i_{Cx}).f_s}{2} \\ \frac{V_{DCM}}{2} + V_{Lx} + \frac{L(i_{Cx(ref)} - i_{Cx}).f_s}{2} \end{bmatrix} \quad (6)$$

In which i_{Cx} is the compensator current through phase x and $i_{Cx(ref)}$ is the current reference value of phase x, V_{x1} and V_{x2} are voltage references of upper and lower HBCCs' legs in phase x respectively. V_{Lx} is the voltage of phase x in the point of common coupling. Also L is the amount of coupling inductance while fs are the switching frequency of the converter.

There are several PWM modulation schemes that could be used with the half bridge cascaded converter. All these PWM modulation schemes have one thing in common. That is to say that each one of the switching commands is generated from the reference signal that is compared with a triangular carrier signal. The intersection points of these two signals will determine the commutation instants. In most cases, in order to achieve a multilevel output voltage, multicarrier PWM strategies are used, i.e., the carrier signals are independent and different in every complementary pair of semiconductors. Therefore, each switching command has an independent carrier, but the reference signal could be shared between different pairs. The so-called "phase-shifted PWM" (PS-PWM) modulation technique is one of these multicarrier PWM strategies, which is used in this paper.

In order to understand the voltage balancing of DC storage capacitors, let's analyze the modulation of one HBM while paying special attention to the DC-link capacitor current and the output voltage. As shown in Fig. 2(B), each HBM consists of a pair of complementary semiconductor branch connected to one DC-link. There are two different combinations depending on the individual switch that is switched on. Clearly, that if the upper switch is on, the output voltage of the HBM would equal to the DC-link voltage. In this condition, positive input current ($i_{xm}>0$) would increase the voltage of the DC capacitor, while negative input current ($i_{xm}<0$) would decrease the voltage of the DC capacitor. Also if the lower switch is on, the output voltage of the HBM would be zero while the capacitor voltage does not change. It is a very important conclusion that is used in the capacitor voltage balancing of each leg.

Thus, the following algorithm is introduced to balance the voltage of DC link capacitors of a leg:

- *If the leg current is positive, then:*

HBM with lower DC-link voltage has to be switched on first.

- *If the leg current is negative, then:*

HBM with higher DC-link voltage has to be switched on first.

According to (3), the modulation signals of upper and lower HBCCs' legs in a phase are of complementary form, but the average active power of both are the same value. To prove this, we can adopt equations (4) and (5), to find the instantaneous power of each HBCC leg in a phase, as below:

$$\begin{bmatrix} P_{x1} \\ P_{x2} \end{bmatrix} = \begin{bmatrix} -\frac{V_{DCM}}{2}(I_{Bx}) - (V_{Lx} + L\frac{di_{Cx}}{2dt}).(\frac{i_{Cx}}{2}) \\ -\frac{V_{DCM}}{2}(I_{Bx}) - (V_{Lx} + L\frac{di_{Cx}}{2dt}).(\frac{i_{Cx}}{2}) \end{bmatrix} + \begin{bmatrix} (V_{Lx} + L\frac{di_{Cx}}{2dt}).(I_{Bx}) + \frac{V_{DCM}}{2}(\frac{i_{Cx}}{2}) \\ -(V_{Lx} + L\frac{di_{Cx}}{2dt}).(I_{Bx}) - \frac{V_{DCM}}{2}(\frac{i_{Cx}}{2}) \end{bmatrix} \quad (7)$$

During one network frequency cycle, the first terms of

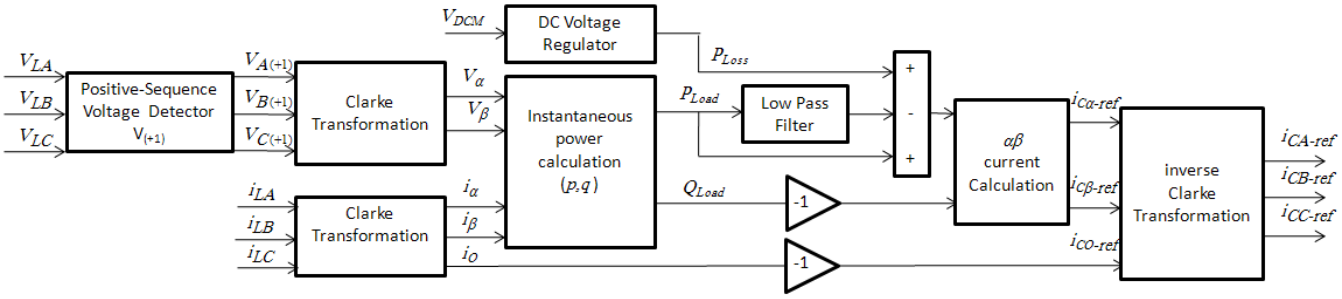

Fig. 3 The control block diagram for the sinusoidal current control strategy

equation (7) have non-zero average values, while the second terms have zero average values. This is because the first terms of the equation are DC components while the second terms are AC components.

Thus, the average value of active power for upper and lower HBCCs' legs connected to the same phase is identical; and hence DC capacitor voltage of the HBMs of both is identical during one network frequency cycle. Due to non-idealistic nature of HBMs, the unbalance of the DC voltage in the upper and lower HBCCs' legs can be eradicated through appropriate adjustment of reference current. In short, through utilization of above techniques, the voltage equality of all DC storage capacitors pertinent to the converter is assured.

To regulate the DC capacitors' voltage to a predetermined reference value, a DC voltage regulator unit is used in the reference current controller as depicted in Fig. 3. Therefore, the average of V_{DCM} is compared with the reference value, and in accordance to their differences, the amount of total input or output active power of the compensator is obtained. It is clear that the value of this active power is in proportion to the converter power losses.

IV. Simulation Results

A ±50*MVA* nine-level type of proposed HBCC-based transformerless STATCOM is simulated using PSIM and MATLAB-SIMULINK concurrently. Power circuit of the compensator is similar to that of Fig. 2(A). With regard to electrical railway application, the network phase voltage amplitude of 25kV is taken as an example. The simulated STATCOM contains three legs in each HBCC, and because of the Software limitations, each of which is comprised of eight HBMs in cascade. All the IGBTs have identical voltage and current ratings. The total number of IGBT modules used for the 25 kV STATCOM is 128. Each HBM has a DC-link (*C=2.35mF*) with a nominal average DC voltage of 10 kV (for the nine-level realization). The capacitance of DC storage capacitor in each HBM is determined on the basis of maximum permitted variations of DC voltage. This value can be calculated by the use of the following equation:

$$C_m = \frac{\int i_m(t).dt}{\Delta V_{Cm}} \qquad (8)$$

In above equation, i_m is the instantaneous current passing through each of the HBMs when we have highest fluctuation of load current, and ΔV_{Cm} is the maximum allowable voltage ripple for DC capacitors. Since the current controller momentarily adjusts the output current of the STATCOM, variation of the DC-links voltages in the permitted region will not cause chaotic state in the compensator operation.

Whenever we get abrupt changes in the load currents, the series filter inductor (*L=3mH*), which is in series with each of the HBCCs' legs of the converter damps the sudden rise of the balancing current I_{Bx}. It will also reduce the output current ripple of the STATCOM. The Inductance of all these inductors is identical and it is calculated according to maximum permitted current ripple of HBCCs' legs. It can be calculated through the following equation:

$$L \cong V_{Cm}\frac{\Delta t}{\Delta i_m} = \frac{V_{DCM}}{(n-1)}.\frac{T_s}{\Delta i_m} = \frac{V_{DCM}}{(n-1).f_s.\Delta i_m} \qquad (9)$$

Where Δi_m is the maximum allowable current ripple in all HBCCs' legs. The PS-PWM modulation technique with a switching frequency of f_s = 1.2 KHz is applied to both HBCCs. The switching frequency is selected upon several factors such as switch types, level of output voltage and allowable THD content of output current.

Fig. 4 shows voltage and current waveforms of the network, load currents, and compensator currents before and after compensation. Reference currents of each phase of converter has been set to zero before *t=0.1*Sec. Therefore load and source currents are similar during this period. Having activated the compensator, the source currents, comprising of load and compensator currents, are balanced to an acceptable value. In other words, source currents do not contain harmonics, while the load currents contain 10% third harmonic. In addition, source currents are in phase with the fundamental of positive sequence voltage and it doesn't contain reactive power components. As shown in Fig. 5, THD of source current is 1.14% which is compatible with IEEE and IEC standards. The compensator absorbs active power by one phase and injects it to other phases, while its DC capacitors' voltages are regulated according to the reference value. Fig. 6 shows DC storage capacitor voltage and output currents of each HBM for upper and lower HBCCs' legs in phase A.

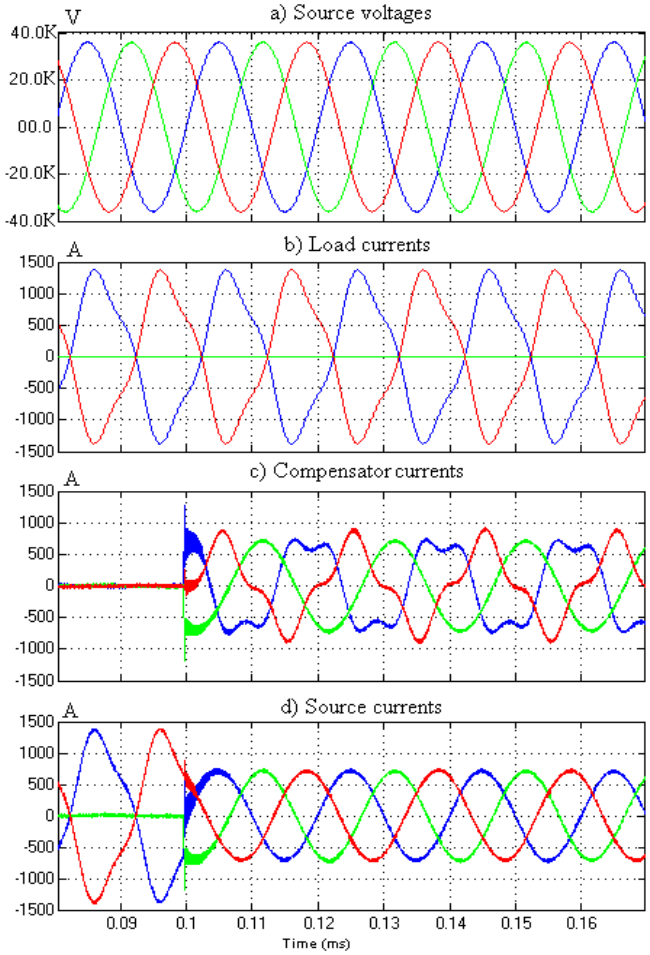

Fig. 4 Voltages and currents before and after compensation

When the output currents of the compensator tend to become unbalanced, the magnitude of HBCCs' currents will increase. In worst conditions, the peak instantaneous HBCCs' currents become equal to the maximum output current of the compensator. This is due to presence of balancing currents in the compensator loops. As the magnitude of load current unbalance decreases, the magnitude of balancing currents will decrease accordingly.

Fig. 7 shows voltage waveforms of upper and lower HBCCs' legs of the converter in phase *A*. As it can be seen, the sum of the voltages of upper and lower HBCCs' legs in each phase is held at V_{DCM} while the voltage of each leg varies from zero to V_{DCM}. Neglecting the inductor voltage of each leg, the voltage between converter phases and neutral point of network will vary from $+V_{DCM}/2$ to $-V_{DCM}/2$, while the line voltage of converter varies from $+V_{DCM}$ to $-V_{DCM}$ during each cycle of network frequency.

On the other hand, as the sum of voltages of upper and lower HBCCs' legs deviate from V_{DCM}, a current will flow from higher voltage HBCCs' legs to lower voltage HBCCs' legs to reduce this difference. The magnitude of this current depends on voltage difference between upper and lower HBCCs. When these currents start to flow, active power will inevitably flow between the compensator phases.

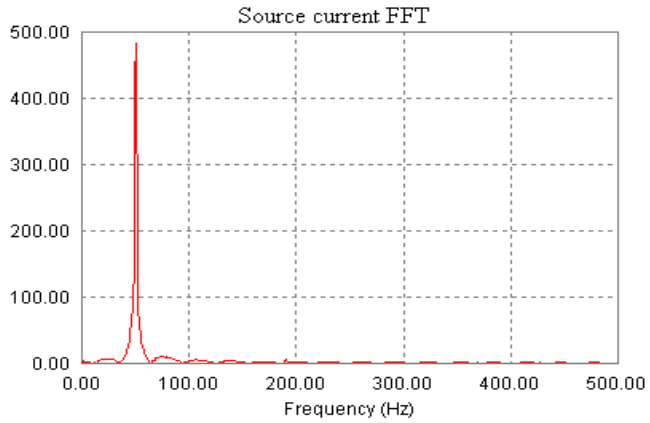

Fig. 5 FFT spectrum of source current after Compensation (THD < 1.14)

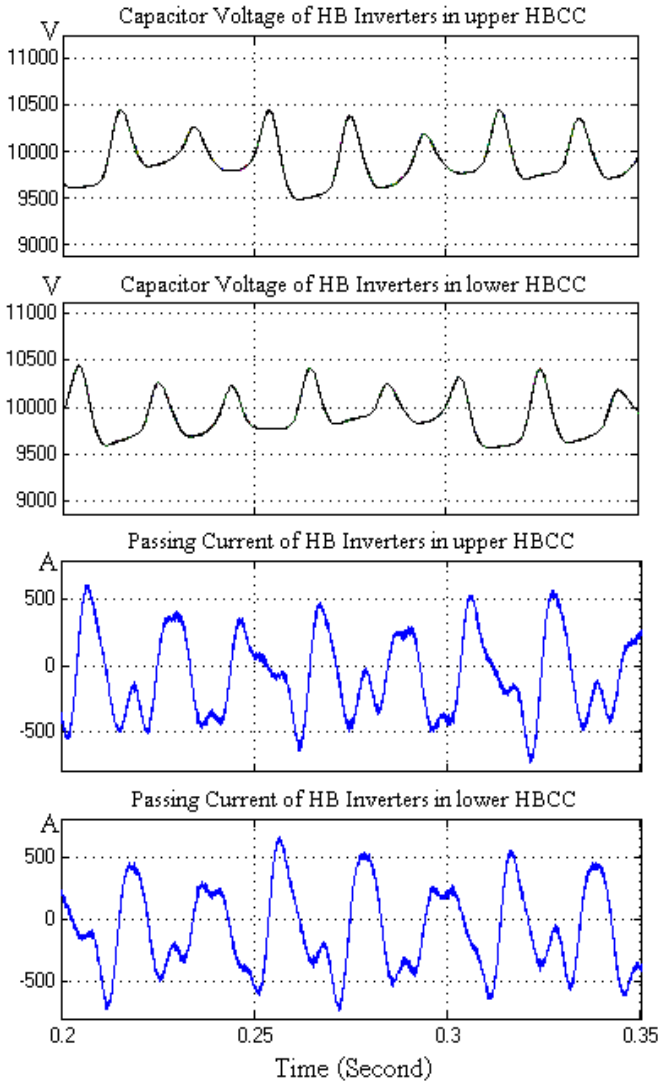

Fig. 6 Capacitor voltages and passing current of HB inverters of upper and lower HBCC in phase *a*

V. Conclusion

In this paper a novel topology has been proposed to compensate the unbalanced and nonlinear medium voltage

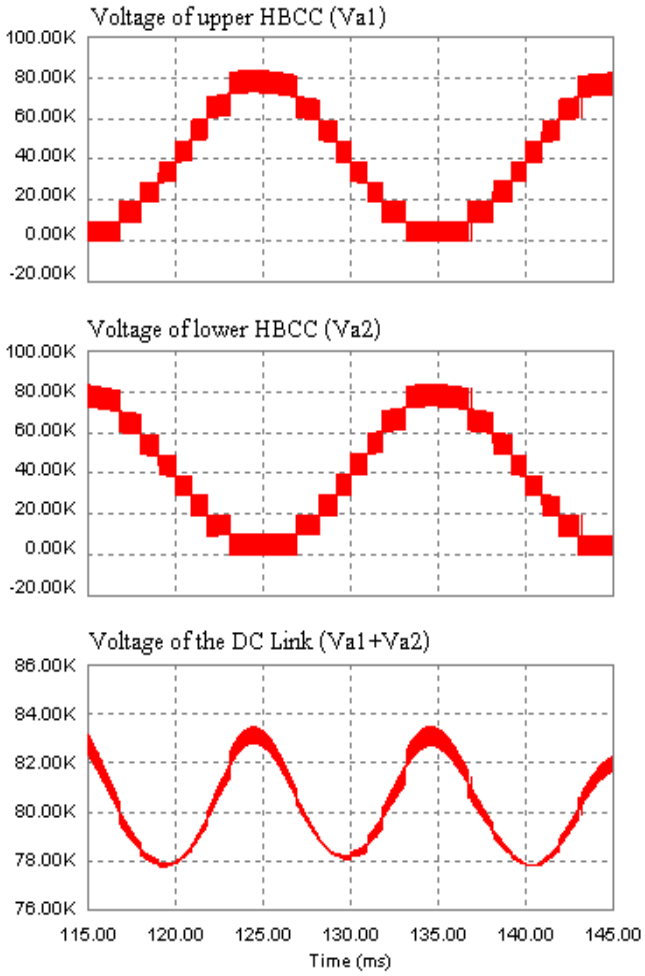

Fig. 7 Voltages of upper and lower HBCCs in phase *A* and the sum of them (V_{DC})

loads under presence of load and source harmonics. The main advantage of this topology is its modularity, compatibility of operation under nonlinear conditions and its ability to work without any low frequency transformer.

Various modular topologies with isolated DC link have been proposed such as cascaded converters with delta or Y connections. But they cannot compensate unbalanced loads with harmonic contents either delta, Y or both. In fact cascaded converters with delta connection cannot possibly inject third harmonic current or compensate neutral current. In Y connected cascaded converters, rebalancing of unbalanced loads is done with some problems. Injection of unbalanced currents by this converter causes injection of active power with non-zero average magnitude from each phase. This will in turn, makes controlling of DC storage capacitor voltages almost impossible.

The proposed modular converter is the developed model of cascaded converter with Y connection that utilizes several isolated units. Each unit comprises a half-bridge-inverter linked to isolated DC capacitors. By utilization of aforementioned controller (part III), all DC capacitors' voltages will be adjusted to a predetermined magnitude. Simulation results prove proper operation of the converter under unbalanced-harmonic conditions.

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