Advanced Non-Inverting Step up/down Converter with LQR Control Technique

Hassan Dehghani[1] , Ali Abedini[2] , Mohammad Tavakoli Bina[3]
[1,2,3]K.N. Toosi University of Technology
[1,2,3]Tehran, Iran
[1]h.dehghani@ee.kntu.ac.ir, [2]abedini@eetd.kntu.ac.ir,[3]tavakoli@eetd.kntu.ac.ir

Abstract—**This paper proposes a new topology of non inverting buck-boost converter. This topology is composed of a boost converter which is followed by a buck converter through a magnetic coupling. A series resistor with capacitor is considered in the boost part to enhance the dynamic of the converter. The advantages of proposed topology are smaller capacitors size, higher bandwith and faster response compared to conventional non inverting buck-boost topologies. Non-ideal DC and AC models of the converter are obtained to analysis the dynamic of the converter with more accuracy. A control algorithm is developed based on LQR method to regulate the output voltage of the converter. This controller is more robust compare to conventional controller. PSCAD/EMTDC software is used to evaluate and verify mathematical model results and simulated circuit model.**

Keywords—Cascade buck-boost converter; LQR control; RHP zeros;Losses; Efficiency.

I. INTRODUCTION

Nowadays, applications of DC-DC converters have been increased significantly because they are widely used in renewable energy systems such as solar systems, fuel cells, battery chargers and etc[1-8].

In many applications due to the large variation of input voltage, step up-down converters must be used. These converters are divided into single inductance i.e. conventional buck-boost converter, or two windings Converter i.e. cascade buck boost groups. Single winding are used to reduce the cost and size of the circuit. However two windings converters are more for high voltage applications where the size of capacitors is more important. Other advantages of two windings converters are the continuous input and output currents, less EMI noises, and better control of input and output currents compared to single winding converters[1].

But the disadvantages of conventional step up-down converters are RHP zeros which restrict the controller response[8,9]. A solution to remove RHP zeros, is using a magnetic coupling between two windings along with a series resistor with capacitor. Moreover this solution helps to gain higher bandwidth and more efficiency[1,9]. This paper proposes a new topology of non inverting buck-boost converter that composed of a boost converter which is followed by a buck converter through a magnetic coupling in order to removing RHP zeros. Also, a series resistor with a capacitor is considered in the boost part to enhance the dynamic of the converter. The control technique which is used in this paper, is LQR to control the proposed converter. LQR control technique has the advantages of more robustness and faster dynamics compared to PI or PID conventional controllers[3].

This paper is organized as follows: Section II introduces proposed converter structure. Section III presents DC and AC mathematical model of the converter. This modeling is carried out considering losses in the windings, power mosfets and diodes. In Section IV elements of the converter is designed step by step. Section V introduce control algorithm for the buck-boost converter. In Section VI a sample buck-boost converter is simulated in frequency domain and time domain. Also, The converter losses and efficiency are calculated. PSCAD/EMTDC is used for simulation. The last section presents the conclusion of this paper.

II. STRUCTURE

Fig. 1 shows the proposed converter circuit diagram. This converter is consisted of a boost converter cascaded with a buck converter. A transformer with turns ratio of 1 is embedded into the boost part, so that the secondary side of transformer is in series with inductor L of the buck part. Also, a damping resistor R_d is in series with the capacitor C in the boost part. C_o and R_o show the filter capacitor and load resistor in the buck part, respectively. V_g shows the input voltage. L_m is the magnetizing inductance of the transformer, R_{on} displays the on resistance of the power mosfets Q_1 and Q_2, and V_D shows the forward voltage drop of the diodes D_1 and D_2. $R_L$illustrates ohmic resistance of the transformer and output inductor.

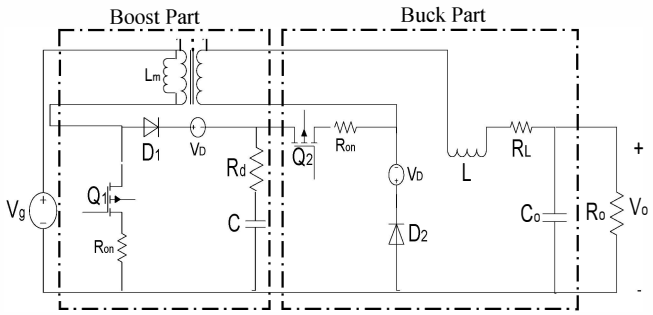

Figure 1. Proposed buck-boost converter topology

III. AC AND DC MODELING

Assume T_S as switching period, Q_1 and Q_2 conduct during $d_1(t)T_s$ and $d_2(t)T_s$ intervals, respectively, while D_1 and D_2 are off in that times. Fig. 2 and Fig. 3 represent the boost and buck modes of the converter, respectively. Assume that the converter operates in continuous conduction mode(CCM), and switching frequency is much higher than the converter natural frequencies[8], the nonlinear state differential equations are as follows:

$$\frac{d\bar{\imath}_{Lm}(t)}{dt} = \frac{\bar{v}_g(t)-d_1(t)\left[R_{on}\left(\bar{\imath}_L(t)+\bar{\imath}_{Lm}(t)\right)\right]-d_1'(t)\left[\bar{v}_C(t)+R_d\bar{\imath}_{Lm}(t)+V_D\right]-d_2'(t)R_d\bar{\imath}_L(t)}{L_m}$$

$$\frac{d\bar{\imath}_L(t)}{dt} = \frac{\bar{v}_g(t)-\bar{v}_o(t)-R_l\bar{\imath}_L(t)-d_1(t)\left[R_{on}\left(\bar{\imath}_L(t)+\bar{\imath}_{Lm}(t)\right)+R_d\bar{\imath}_L(t)-\bar{v}_C(t)\right]}{L} + \frac{-d_1'(t)(R_{on}\bar{\imath}_L(t)+V_D)-d_2'(t)\left[R_d\left(\bar{\imath}_L(t)+\bar{\imath}_{Lm}(t)\right)+\bar{v}_C(t)+V_D-R_{on}\bar{\imath}_L(t)\right]}{L}$$

$$\frac{d\bar{v}_C(t)}{dt} = \frac{-d_1(t)\bar{\imath}_L(t)+d_1'(t)\bar{\imath}_{Lm}(t)+d_2'(t)\bar{\imath}_L(t)}{C}$$

$$\frac{d\bar{v}_o(t)}{dt} = \frac{\bar{\imath}_L(t)}{C_o}-\frac{\bar{v}_o(t)}{\bar{R}_oC_o} \quad (1)$$

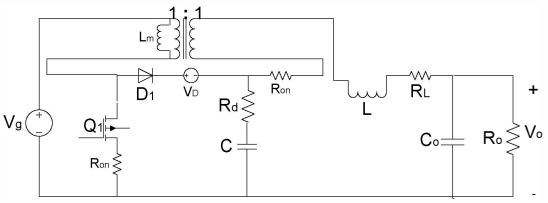

Figure 2. The boost mode of the converter

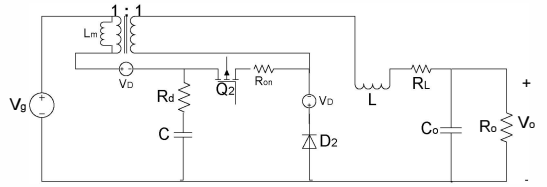

Figure 3. The buck mode of the converter

Where $\bar{z}_j$ is mean of the z_j in the switching period T_s, where z_j is any variable i.e. v_g,i_L,d_1,... :

$$\bar{z}_j = Z_j + \hat{z}_j \quad (2)$$

Where the Z_j is the DC part of z_j, and $\hat{z}_j$ is the ac part of it, around Z_j. By substituting (2) in (1) and separating the ac part from the DC part, the operating point of the converter is gained as following:

$$V_o = \left(\frac{D_2}{D'_1}V_g - V_D\right)\frac{1}{1+\left(\frac{D_2}{D'_1}-1\right)^2\frac{R_1}{R_o}+\frac{R_2}{R_o}}$$

$$I_L = \frac{V_o}{R_o}$$

$$I_{L_m} = \left(\frac{D_2}{D'_1}-1\right)I_L$$

$$V_c = \frac{V_g-R_1I_{L_m}-D'_1V_D}{D'_1} \quad (3)$$

Where in the above terms R_1 and R_2 are as follows:

$$R_1 = \left(\frac{D_1D_2}{D_2-D'_1}\right)R_{on} + \left(\frac{D_1D'_1}{D_2-D'_1}\right)R_d$$

$$R_2 = \left(D'_1 + D'_2 + \frac{D_1D_2}{D'_1}\right)R_{on} + \left(D_1 + \frac{D_2D'_2}{D'_1}\right)R_d + R_l \quad (4)$$

Considering $\hat{x}$ as the ac state vector of the converter, then:

$$\hat{x} = \left[\hat{\imath}_{L_m}\ \hat{\imath}_L\hat{v}_C\ \hat{v}_o\right]^T \quad (5)$$

the small signal model of the converter is equation (6).

$$\frac{d\hat{x}}{dt} = A\hat{x} + B_1\hat{d}_1 + B_2\hat{d}_2 + B_3\hat{v}_g + B_4\hat{r}_o \quad (6)$$

Where ,B_1, B_2, B_3 and B_4 are as follows:

$$A = \begin{bmatrix} \frac{-(D_1R_{on}+D'_1R_d)}{L_m} & \frac{-(D_1R_{on}+D'_2R_d)}{L_m} & -\frac{D'_1}{L_m} & 0 \\ \frac{-(D_1R_{on}+D'_2R_d)}{L} & \frac{-(D_2R_{on}+(D_1+D'_2)R_d+R_l)}{L} & \frac{D_2-D'_1}{L} & -\frac{1}{L} \\ \frac{D'_1}{C} & \frac{D'_2-D_1}{C} & 0 & 0 \\ 0 & \frac{1}{C_o} & 0 & \frac{-1}{R_oC_o} \end{bmatrix}$$

$$B_1 = \left[\frac{(V_c+R_dI_{L_m}+V_D-R_{on}I_g)}{L_m}\ \frac{(V_c+V_D-R_{on}I_{L_m}-R_dI_L)}{L}\ \frac{-I_g}{C}\ \ 0\right]^T$$

$$B_2 = \left[\frac{R_dI_L}{L_m}\ \frac{(V_c+V_D-R_{on}I_L+R_dI_g)}{L}\ \frac{-I_L}{C}\ \ 0\right]^T$$

$$B_3 = \left[\frac{1}{L_m}\ \frac{1}{L}\ \ 0\ \ 0\right]^T$$

$$B_4 = \left[0\ \ 0\ \ 0\ \ \frac{I_L}{R_oC_o}\right]^T \quad (7)$$

In the above terms, $I_{L_m} + I_L = I_g$, is the converter input current. Fig. 4 and Fig. 5 illustrate DC and ac small signal transformer model of the proposed converter, respectively. In the ac model, α and β are as follows:

$$\alpha = V_c + V_D - R_{on}I_g + D'_1R_dI_g - D_2R_dI_L$$

$$\beta = V_c + V_D - R_{on}I_L + D'_1R_dI_g - D_2R_dI_L \quad (8)$$

The voltage conversion ratio is gained as follow:

$$M \equiv \frac{V_o}{V_g} = \left(\frac{D_2}{D'_1}-\frac{V_D}{V_g}\right)\frac{1}{1+\left(\frac{D_2}{D'_1}-1\right)^2\frac{R_1}{R_o}+\frac{R_2}{R_o}} \quad (9)$$

Fig. 6 shows M as function of D_1+D_2 , as shown M is a continuous curve between the boost and buck modes of operation.

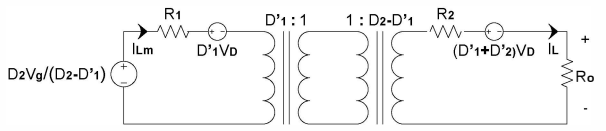

Figure 4. DC transformer model of the converter

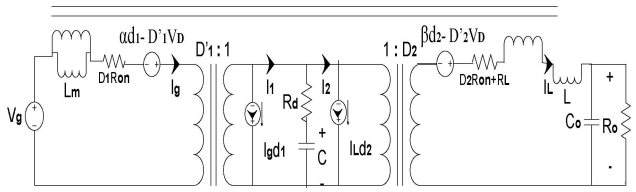

Figure 5. ac transformer model of the converter

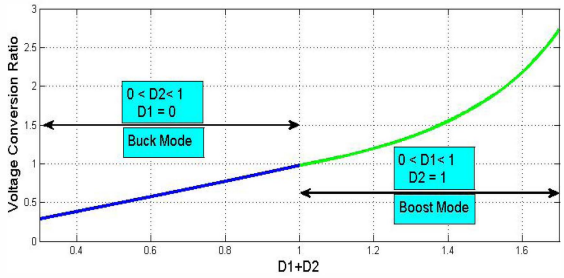

Figure 6. Voltage conversion ratio M, as function of D_1+D_2

IV. DESIGNING ELEMENTS OF THE CONVERTER

Output Inductor(L) Selection

inductor L is calculated as follow:

$$L = Max\{L_1, L_2\} \tag{10}$$

Where L_1 and L_2 are:

$$L_1 = \frac{-(V_g - V_D - R_{on}I_L - R_lI_L - V_o)D'_1T_s}{\Delta i_{L_{Boost}p-p}}$$

$$L_2 = \frac{(V_g - V_D - R_{on}I_L - R_lI_L - V_o)D_2T_s}{\Delta i_{L_{Buck}p-p}} \tag{11}$$

In the above equations, $\Delta i_{L,Boost,p-p}$ and $\Delta i_{L,Buck,p-p}$ are peak to peak output inductor current ripples in the boost and buck modes respectively.In the each mode, with regard to maximum value of these current ripples, minimum value for L_1 and L_2must be selected separately, in order to obtaining CCM conditions for current of the output inductor L.

MagnetizingInductor(L_m) Selection

Magnetizing inductor $L_m$is gained of:

$$L_m = Max\{L_{m_1}, L_{m_2}\} \tag{12}$$

Where L_{m_1} and L_{m_2} are:

$$L_{m_1} = \frac{(V_g - R_{on}I_g)D_1T_s}{(\Delta i_{g_{Boost}p-p} - \Delta i_{L_{Boost}p-p})}$$

$$L_{m_2} = \frac{(V_g - V_D - R_dI_{Lm} - V_c)D_2T_s}{(\Delta i_{g_{Buck}p-p} - \Delta i_{L_{Buck}p-p})} \tag{13}$$

In the last equations, $\Delta i_{L_m,Boost,p-p}$ and $\Delta i_{L_m,Buck,p-p}$ are peak to peak magnetizing inductor current ripples in the boost and buck modes respectively. L_m is determined with regard to the maximum allowed of the input current ripple.

Output Capacitor(C_o) Selection

Capacitor C_o is calculated as follow:

$$C_o = Max\{C_{o_1}, C_{o_2}\} \tag{14}$$

Where C_{o_1} and C_{o_2} are:

$$C_{o_1} = \frac{\Delta i_{L_{Boost}p-p}T_s}{8\Delta v_{o_{Boost}p-p}} \quad , C_{o_2} = \frac{\Delta i_{L_{Buck}p-p}T_s}{8\Delta v_{o_{Buck}p-p}} \tag{15}$$

In above equations, $\Delta v_{o,Boost,p-p}$ and $\Delta v_{o,Buck,p-p}$ are peak to peak output capacitor voltage ripples in the boost and buck modes respectively. C_{o1} and C_{o2} are determined with regard to the maximum allowed output voltage ripples.

Input Capacitor(C) and Damping Resistor(R_d)

Selecting values of L, L_m and C_o is accomplished with regard to desired peak to peak their current and voltage ripples. But C and R_d determine the location of the converter zeros and converter dynamic. Therefore they must be selected so that the zeros are in the left half plane(LHP) with good dynamic converter response.

The output transfer function of the converter based on Fig. 3 is this:

$$G_{\hat{v}_o\hat{d}_1}(s) = \frac{\hat{v}_o(s)}{\hat{d}_1(s)} = \frac{a_2s^2 + a_1s + a_0}{b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0} \tag{16}$$

Where:

$$a_0 = D'_1R_o(V_c - R_dI_L) \tag{17}$$

$$a_1 = D'_1R_dCR_o(V_c - R_dI_L) - D_1L_mR_o(I_L + I_{L_m}) \tag{18}$$

$$a_2 = L_mCR_o(V_c - R_dI_L) \tag{19}$$

$$b_0 = D'^2_1R_o + D_1D'_1R_d$$
$$b_1 = D_1^2L_m + D'^2_1L + D_1D'_1R_dR_oC_o + D'_1R_dD'_1R_d + D_1D'_1R_d^2C$$
$$b_2 = D_1^2L_mR_oC_o + D'^2_1LR_oC_o + D_1D'_1R_d^2C + D_1L_mR_dC + D'_1R_dLC + L_mCR_o$$
$$b_3 = L_mLC + D_1L_mR_dCR_oC_o + D'_1R_dCLR_oC_o$$
$$b_4 = L_mLCR_oC_o \tag{20}$$

To eliminate RHP zeros the following conditions must be met:

$$a_0 > 0,\ a_1 > 0\ ,\ a_2 > 0 \tag{21}$$

Having $a_0 > 0$ and $a_2 > 0$, with respect to (3) must be following condition satisfied:

$$R_d < R_o \tag{22}$$

Having $a_1 > 0$, since $I_o = I_L$, by replacingit in (18), and using (3), then:

$$a_1 = R_dCR_oV_g - (R_d^2CR_o + \frac{D_1}{D'_1}L_mR_o)I_o \tag{23}$$

Considering (23), as shown in Fig. 7, $I_{o_{Critical}}$ is defined as where $a_1 = 0$, then:

$$I_{o\,Critical} = \frac{R_d C V_g}{{R_d}^2 C + \frac{D_1}{D'_1} L_m} \quad (24)$$

To have all zeros in LHP, the following conditions must be met:

$$I_o = \frac{V_g}{D'_1 R_o + D_1 R_d} < I_{o\,Critical} = \frac{R_d C V_g}{{R_d}^2 C + \frac{D_1}{D'_1} L_m} \quad (25)$$

$${R_d}^2 - R_o R_d + \frac{D_1 L_m}{{D'_1}^2 C} = \rho(R_d) < 0 \quad (26)$$

$$\frac{R_o}{2} - \frac{1}{2}\sqrt{{R_o}^2 - \frac{4 D_1 L_m}{{D r_1}^2 C}} < R_d < \frac{R_o}{2} + \frac{1}{2}\sqrt{{R_o}^2 - \frac{4 D_1 L_m}{{D r_1}^2 C}} \quad (27)$$

According (27) must:

$${R_o}^2 - \frac{4 D_1 L_m}{{D'_1}^2 C} > 0 \quad (28)$$

Then:

$$C > \frac{4 D_1 L_m}{{D'_1}^2 {R_o}^2} \quad (29)$$

By taking derivative of (24) with respect to R_d and equaling to zero, $R_{d_{opt}}$ is achieved as follow:

$$R_{d_{opt}} = \sqrt{\frac{D_1 L_m}{D'_1 C}} \quad (30)$$

Fig. 8 illustrates $I_{o_{Critical}}$ as function of the R_d for different values of the duty cycle D_1.

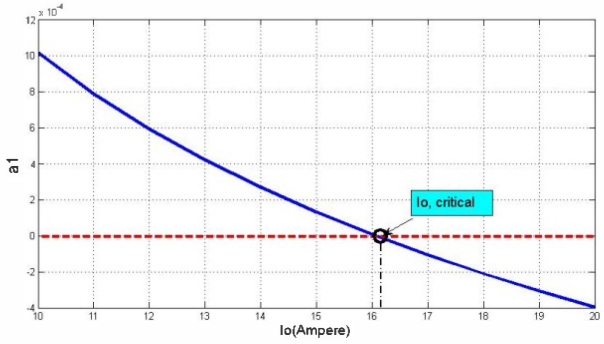

Figure 7. Coefficient a_1 asfunction of I_o

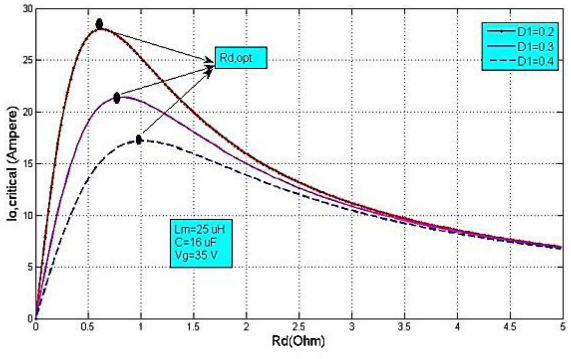

Figure 8. $I_{o_{Critical}}$ as function of the R_d for different values of the duty cycle D_1 and showing $R_{d_{opt}}$ in the each them

V. CONTROLALGORITHM

LQR control techniqueis used to design the control algorithm of the proposed converter. The theory of optimal control is concerned with operating a dynamic system at minimum cost. The case where the system dynamics are described by a set of linear differential equations and the cost is described by a quadratic functional is called the LQ problem. One of the main results in the theory is that the solution is provided by the linear-quadratic regulator (LQR)[10]. If the state equations of the system are these:

$$\dot{x} = Ax + Bu$$
$$y = Cx + Du \quad (31)$$

By using LQR:

$$u = -Kx \quad (32)$$

Where matrix K must be selected so that, J is minimized:

$$J = \int_0^\infty (x^T Q x + u^T R u)\,dt \quad (33)$$

Where J is the cost function which must be minimized and Q(state weighting matrix)$\geqslant$ 0 and R(inputweighting matrix) > 0.

K is gained as follows:

$$K = R^{-1} B^T P \quad (34)$$

And P is obtained via the following algebraic ricatti equation:

$$A^T P + PA + -PBR^{-1} B^T P + Q = 0 \quad (35)$$

Fig. 9 illustrates the control block diagram of the converter. As shown, because the system type is zero, an integrator must be used to have zero steady-state error.

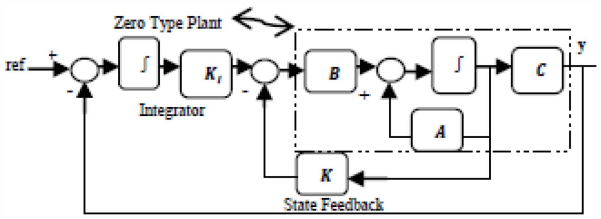

Figure 9. control block diagram for converter

Q and R are selected as:

$$Q = \begin{bmatrix} Q_{i_{Lm}} & 0 & 0 & 0 \\ 0 & Q_{i_L} & 0 & 0 \\ 0 & 0 & Q_{\hat{v}_c} & 0 \\ 0 & 0 & 0 & Q_{\hat{v}_o} \end{bmatrix}$$

$$R = \begin{bmatrix} R_{\hat{d}_1} & 0 \\ 0 & R_{\hat{d}_2} \end{bmatrix} \quad (36)$$

And K is this:

$$K = \begin{bmatrix} K_{11} & K_{12} & K_{13} & K_{14} \\ K_{21} & K_{22} & K_{23} & K_{244} \end{bmatrix} = \begin{bmatrix} \boldsymbol{K_1} \\ \boldsymbol{K_2} \end{bmatrix} \quad (37)$$

Thus the closed-loop system representation is given by:

$$A_c = A - B_1K_1 - B_2K_2 \qquad (38)$$

Where in that, A_c is new state matrix of the converter.

VI. SIMULATIONRESULTS

In this paper a case study has been accomplished. Simulation of the buck-boost converter has been considered for the design parameters which are mentioned in table I. By using equations given previously in the paper the elements values are obtained in table II. There are 3 columns in table II: boost mode, buck mode and final selection. The boost and buck modes columns show the obtained value of the elements in the boost and buck modes respectively, and the final selection is made based on the worst case conditions. Table III shows input parameters of the converter shown in Fig. 1. Assuming as follows:

$$Q_{\hat{i}_{Lm}} = 0,\ Q_{\hat{i}_L} = 0,\ Q_{\hat{v}_c} = 0,\ Q_{\hat{v}_o} = 0.03$$
$$R_{\hat{d}_1} = R_{\hat{d}_2} = 1 \qquad (39)$$

K is gained as follows:

$$K_{11} = 0,\quad K_{12} = 0.0291,\quad K_{13} = 0,\quad K_{14} = 0.1062$$
$$K_{21} = 0,\quad K_{22} = 0.0340,\quad K_{23} = 0,\quad K_{24} = 0.1242 \qquad (40)$$

K_I as an integrator coefficient according Fig. 9, is achieved in order that cut off frequency of the open loop transfer function be a twentieth of the switching frequency($\omega_C = 31400$) .

$$\left|\frac{K_I}{(j\omega)} G_{\hat{v}_o\hat{d}}(j\omega)\right|_{D_1=0,D_2=1\&\omega_C=31400} = 1 = 0\ db$$
$$K_I = 8102 \qquad (41)$$

Fig. 10 and Fig. 11 illustrate Voltgaes and currents of the converter in the boost(V_g=35V) and buck(V_g=65V) modes, respectively.

A. *Converter analysis results in MATLAB software*

In this section, the time and frequency domain performance of the proposed converter is investigated. Fig. 12 illustrates step response of the proposed converter in the boost and buck modes. As shown, the system responds quickly with little overshoots, and zero steady-state errors and the short settling times in the both modes, but the overshoot and settling time in the boost mode is more than the buck mode. Fig. 13 illustrates bode diagram of the proposed converter in the boost and buck modes. As shown, Desirable phase margin(about 60◦), and cut-off frequency(about 5kHz), is obtained with used control algorithm.

B. *Losses and efficiency calculation of converter*

The conduction losses of the converter regardless of the equivalent series resistance (ESR) of the capacitor is obtained as following equation:

$$P_{Loss,Cond} = R_l {I_{L,rms}}^2 + R_{on}\left({I_{Q_1,rms}}^2 + {I_{Q_2,rms}}^2\right) + R_d {I_{C,rms}}^2 + V_D\left(I_{D_1,rms} + I_{D_2,rms}\right) \qquad (42)$$

The converter switching losses which is due to the switching of the power MOSFETS, are obtained as follows:

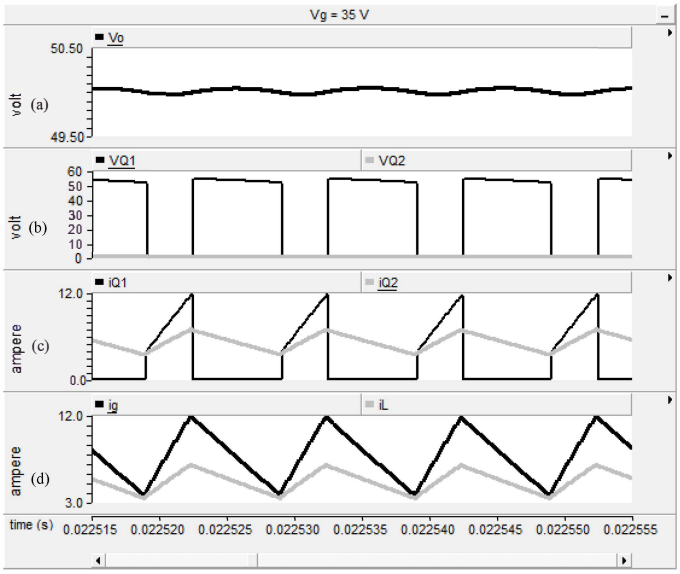

Figure 10. Voltgaes and currents of the converter in the boost mode(V_g=35V)(a):output voltage; (b):voltage of Q_1 with black color and voltage of Q_2 with gray color; (c):current of Q_1 with black color and current of Q_2 with gray color; (d): i_g with black color and i_L with gray color.

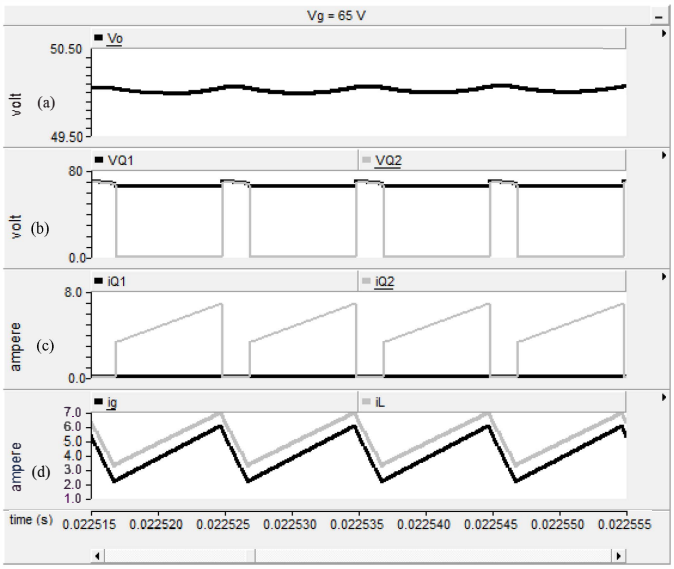

Figure 11. Voltgaes and currents of the converter in the buck mode(V_g=65V)(a):output voltage; (b):voltage of Q_1 with black color and voltage of Q_2 with gray color; (c):current of Q_1 with black color and current of Q_2 with gray color; (d): i_g with black color and i_L with gray color.

$$P_{Loss,Sw_{Q_1}} = P_{on,Sw_{Q_1}} + P_{off,Sw_{Q_1}} =$$
$$\frac{f_s}{2}\left(V_{Q_1,min} I_{Q_1,min} t_r + V_{Q_1,max} I_{Q_1,max} t_f\right) \textbf{Boost Mode} \qquad (43)$$
$$P_{Loss,Sw_{Q_2}} = P_{on,Sw_{Q_2}} + P_{off,Sw_{Q_2}} =$$
$$\frac{f_s}{2}\left(V_{Q_2,min} I_{Q_2,min} t_r + V_{Q_2,max} I_{Q_2,max} t_f\right) \quad \textbf{Buck Mode} \qquad (44)$$

Total losses of the converter is as follows:

$$P_{Losses} = P_{Loss,Cond} + P_{Loss,Sw} \qquad (45)$$

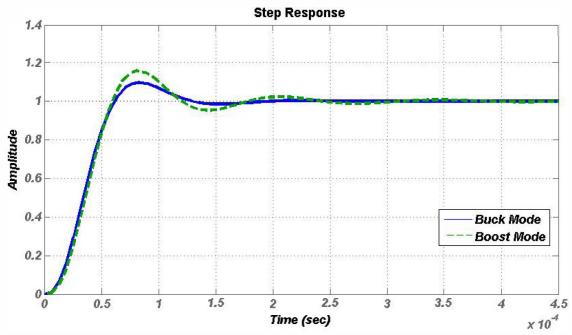

Figure 12. The Step responses of the proposed converter in the boost and buck modes

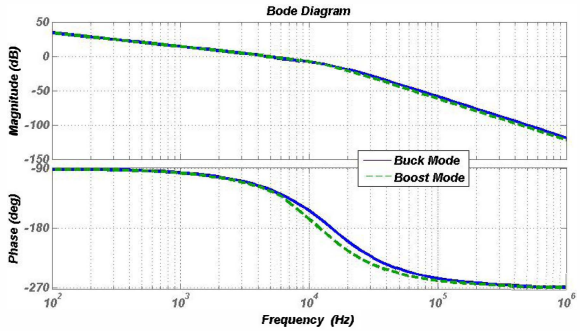

Figure 13. Bode diagram of the converterin the boost and buck modes

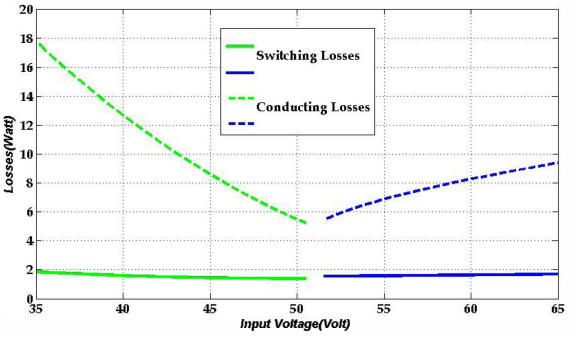

Figure 14. The converter conduction and switching losses as function of the input voltage

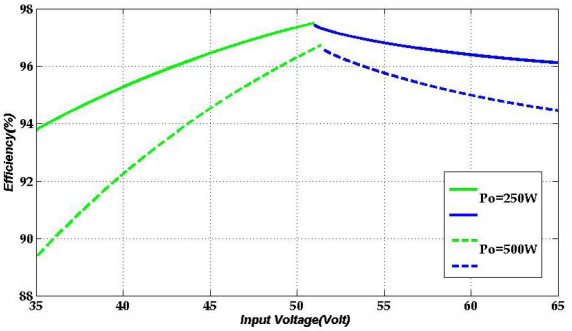

Figure 15. The converter efficiency as function ofthe input voltage for the nominal and maximum loads

And finally, efficiency of the buck-boost converter is:

$$\eta_{Converter} = \frac{P_{in} - P_{Losses}}{P_{in}} \qquad (46)$$

Where $P_{in} = V_g I_{g,rms}$. Fig. 14 represents the conduction and switching losses, and Fig. 15 represents the efficiency of the converter as functions of the input voltage, in the boost and buck modes.

TABLE I. THE CONVERTER DESIGN PARAMETERS

$V_g = 35V \sim 65V$	Input voltage range
$V_o = 50V$	Reference value of the output voltage
$\Delta v_{o_{p-p}} = 0.16V_o$	peak to peak output voltage ripple
$\Delta i_{g_{p-p}} = 9A$	peak to peak input current ripple
$\Delta i_{L_{p-p}} = 4A$	peak to peak inductor L current ripple
$P_{o,max} = 500W$, $P_{o,rated} = 250W$	Nominal and Maximum output power
$f_s = 100kHZ$	Switching frequency

TABLE II. THE CONVERTER CIRCUIT ELEMENTS VALUES

Element	***Boost mode***	***Buck mode***	***Final selection***
Magnetizing inductor	$L_{m_1} = 23.86\mu H$	$L_{m_2} = 18.47\mu H$	$L_m = 25\mu H$
Output inductor	$L_1 = 26.32\mu H$	$L_2 = 27.8\mu H$	$L = 30\mu H$
Output capacitor	$C_{o_1} = 62.5\mu F$	$C_{o_2} = 62.5\mu F$	$C_o = 66\mu F$
Input capacitor	$C_1 = 17.1\mu F$	$C_2 = 8.3\mu F$	$C = 16\mu F$

TABLE III. VALUES AND TYPE OF THE CONVERTER CIRCUIT ELEMENTS

Element	***Symbol(type)***	***Quantity***
Damping resistor	R_d	$0.8\ \Omega$
Transformer and output inductor ohmic resistance	R_L	$70\ m\Omega$
Power mosfet	Q_1&Q_2 IRFB4115PbF	$\boldsymbol{t_r = 73ns}$ $\boldsymbol{t_f = 39ns}$ $\boldsymbol{R_{on} = 10m\Omega}$
Schottky diode	D_1&D_2 40CPQ080G	$\boldsymbol{V_D = 0.6V}$

C. Converter simulating results in PSCAD/EMTDC software

Simulating is accomplished with considering 1 microsecond delay time to make gate signals u_1 and u_2. Fig. 16 shows the case which the input voltage changes from 35V to 65V, with frequency of 50Hz, at nominal load. This test is done to evaluate the dynamic stability of the proposed converter, and respond of the designed control to such small signal disturbances. As shown, in the both boost and buck modes, gates signal u_1 and u_2 are made correctly, so that the output

voltage is regulated at 50V in the allowed ripple range. Fig. 17 and Fig. 18show the casesin which the converter is on the minimum input voltage(35V) in the boost mode and the maximum input voltage(65V) in the buck mode, respectively. Suddenly, load resistor changes from 10Ω to 5Ω and after a short time returns to the original state. These tests done to evaluate transient stability of the proposed converter to these large signal perturbations. As shown in the both modes, the designed controller regulates the output voltage in the reference value,among allowed ripple range with appropriate overshoot and settling time similar to step response of Fig. 12.

I. CONCLUSION

A new non-inverting step up/down converter topology is discussed here. LQR technique is applied to regulate the output voltage of the converter. The DC model and dynamic model of the converter are gained to compare the performance of the converter with conventional converter. The Dynamic model showed that there is no any RHP zero in the transfer function of the proposed converter. Simulation results also match closely with the responses of mathematical model gained in MATLAB. Finally the losses calculation shows that the efficiency has not been scarified in this converter compared to conventional converter.

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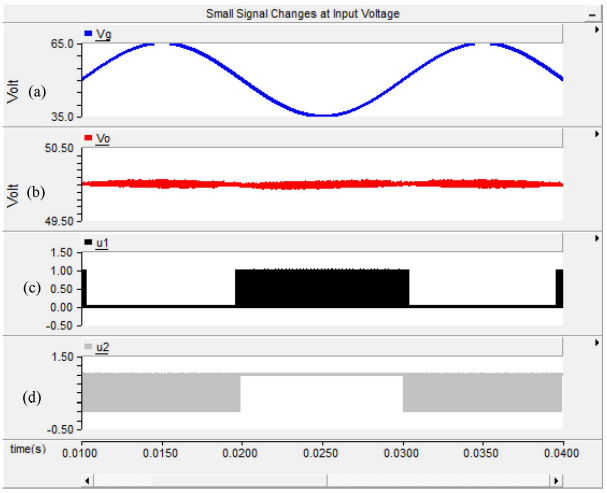

Figure 16. Changing the input voltage at nominal load, and keeping output voltage in the allowed range for converter dynamic stability evaluation; (a):input voltage; (b):output voltage; (c):gate signal u_1; (d):gate signal u_2

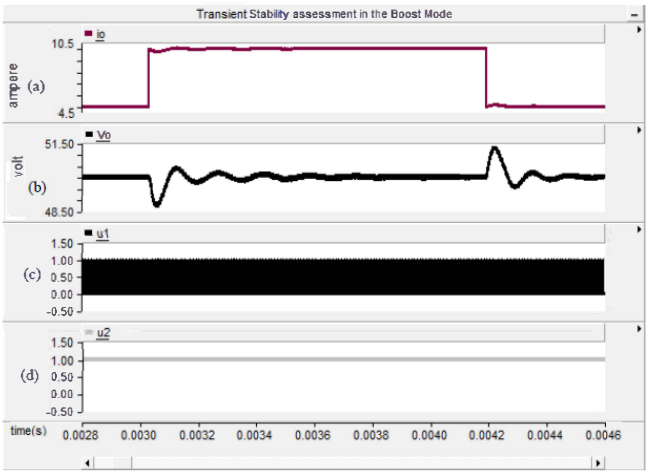

Figure 17. Converter transient stability evaluationin the boost mode(V_g=35V) (a): load current ; (b): output voltage; (c): gate signal u_1; (d):gate signal u_2

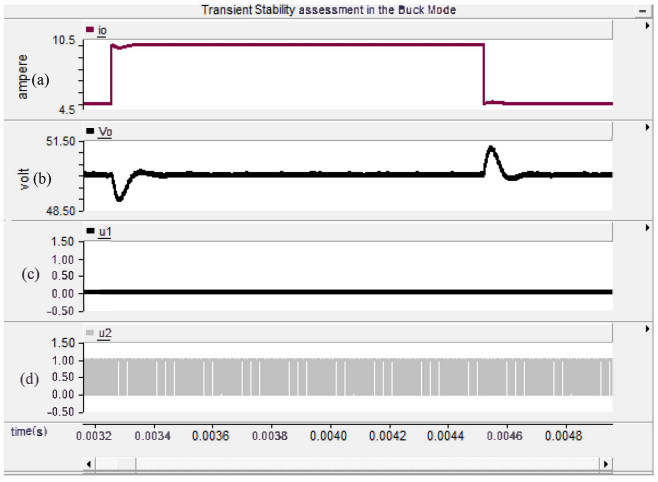

Figure 18. Converter transient stability evaluation in the buck mode(V_g=65V) (a):load current ; (b):output voltage; (c):gate signal u_1; (d):gate signal u_2