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An Optimized Variable-offset Modulation Technique for Three-phase Differential Multilevel Converters

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***Abstract*—In recent years many different modulation techniques have been introduced in order to support the growing number of multilevel converter topologies. These techniques have own disadvantages and some limitations. This paper presents a new optimized variable offset modulation technique for differential multilevel converters. The proposed modulation technique with achievement to full DC utilization reduces switching losses. For a comprehensive analysis the optimized offset has been compared with three conventional modulation techniques. Modeling and analysis are first introduced for a buck converter, and then are expanded to a general differential three phase multilevel converter. Furthermore, simulation verification are taken place on a 16 level cascaded multilevel converter in order to confirm the introduced technique as well as theoretical analysis. Simulations results verify the introduced modulation techniques.**

Keywords—differential multilevel converter; fix offset; optimized offset; asymmetric multilevel converter

I. INTRODUCTION

Multilevel converters with high number of voltage levels can generate high quality voltage waveforms, with good enough THD. So they can be considered as suitable voltage generators in power application like smart grid with various power supplies [1]. Another advantage of such converters is their ability to synthesize waveforms with higher voltage levels, introducing a solution to increase the converter operating voltage above the voltage limits of classical semiconductors [2]. The multilevel converter are recently applied at many industrial applications such as ac power supplies, wind power, FACTS, distribution generation, drive systems and HVDC [1]. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources such as photovoltaic, wind, and fuel cells that are connected to grid for high power applications [3-4].

Many new modulation techniques have been developed to support the growing number of multilevel converter topologies [1]. These modulation techniques have own disadvantages and some limitations. A modulation technique affects switching losses, the THD as well as optimal usage of the DC-link [5]. The main objective of this article is to find an efficient modulation technique for multilevel converters. Modeling and analysis of multilevel converters in form of three independent DC-DC multilevel buck-converter and using basic equations of buck converter lead to an optimized modulation technique. Performance of the proposed optimized offset modulation technique is compared with those of the common techniques in [5-9] such as fix offset, third harmonic injection PWM (THIPWM) and the SVPWM. The common aspect of these methods is the ability of running with carrier base switching techniques. Shifted level PWM (LS-PWM) [10] switching technique is used to run four modulation techniques on a differential three phase 16-level converter for comprehensive comparison. Analysis the obtained results indicate that applying the optimized offset modulation on multilevel converter leads lower switching losses, better THD as well as optimal usage of the DC-link.

II. MODULATING THREE-PHASE MULTILEVEL CONVERTER

Consider the DC-DC buck converter shown in Fig. 1(a). In order to use a number of lower-voltage sources, DC input section similar to Fig. 1(b) can be replaced with m 2-level choppers which have similar duty cycle. In this case, all dc voltage sources are equal and in accordance with (1) the total voltage of them are equal to V_{DC}. Also, if the voltage sources of the choppers are not equal (asymmetric), it is possible to find more voltage level by choosing the correct voltage source ratio like asymmetric Binary or Trinary ratio [11]. With a duty cycle like (2) the buck converter shown in Fig. 1(a) is able to produce a sinusoidal voltage with a DC offset by using the usual 2-level PWM method.

$$V_1 = V_i = V_{dc} \qquad \text{i=2,..., m}$$
$$\mathrm{V}_{DC} = \sum_{i=1}^{m} V_i = m \times V_{dc} \tag{1}$$
$$D_1(t) = D_2(t) = \ldots = D_m(t) = D(t)$$

$$\begin{cases} V_{aN} / V_{DC} = D(t) = A\sin(\omega t) + A \\ 0 \le \mathrm{D(t)} \le 1 \quad \Rightarrow \quad \mathrm{A} \le 0.5 \end{cases} \tag{2}$$

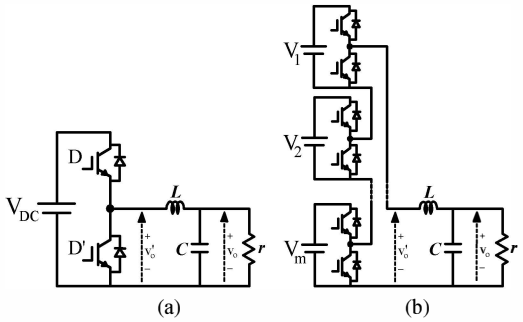


Figure 1. (a) a conventional DC-DC buck converter, (b) expanded model of the conventional buck.

The expanded converter shown in Fig. 1(b) by using a multilevel PWM methods such as LS-PWM techniques [10] or Fundamental switching frequency [12] will be able to produce sinusoidal voltage with positive levels (along with a DC offset). In this case the input voltage to the low-pass filter LC in 2-level buck converter is converted to a multilevel one that would reduce the size of the output filter, switching frequency and losses. So the converter shown in Fig. 1(b) can be considered as a multilevel buck-converter that able to generate sinusoidal multilevel voltage waveform with a DC offset.

By combining of three buck converter as shown in Fig. 2(a) with differential topology can be found a three phase inverter. The load-voltage is cased from difference of two phase voltages that due to the DC offset is equal to all phases, no average voltage can be applied to load. Such a discussion would also include for the described multilevel buck-converter with difference that the DC sources used for each phase exception of the lowest chopper should be isolated. Such three phase differential multilevel converter is shown in Fig. 2 (b).

III. Applying Different Modulation Techniques On Three-Phase Multilevel Converters

Several modulation techniques like sinusoidal carrier based methods and SVM are usual for multilevel converters. Carrier based methods because of their simplicity in implementation are more usual [1] but they have a big disadvantage with modulation index limitation [5]. This section introduces a Fix offset and two variable offset modulation technique for three phase differential multilevel converters. Also the optimized offset modulation technique will be proposed.

A. Fixed offset carrier base sinusoidal modulation technique

Consider the three-phase differential buck-converter shown in Fig. 2 (a). A simple solution for the inverter modulation is the production of three independent carrier base sinusoidal PWM with 120º phase shift at any phase. In order to usage of fix offset modulation technique, it can be added a fixed amount equal to sinusoidal waveform amplitude according (3) for production of three sine waveform at three-phase buck-converter output [5].

$$\begin{cases} V_{aN}/V_{DC} = D_a(t) = A\sin(\omega t) + A \\ V_{bN}/V_{DC} = D_b(t) = A\sin(\omega t + 2\pi/3) + A \\ V_{cN}/V_{DC} = D_c(t) = A\sin(\omega t - 2\pi/3) + A \\ 0 \le D(t) \le 1 \quad \Rightarrow \quad A \le 0.5 \end{cases} \tag{3}$$

$$D(t) = \sum_{i=1}^{m} V_i \times d_i / V_{DC}\ , \quad V_{DC} = \sum_{i=1}^{m} V_i \tag{4}$$

Equation (3) can also be considered for the multilevel converter shown in Fig. 2 (b) with difference that all chopper duty cycle are different from each other and total duty cycle ($D(t)$) is obtained from (4). In (4) V_i and d_i are dc voltage source and duty cycle of the ith chopper respectively.

Due to the duty cycle limitation between 0 and 1 the DC offset value A is limited to a maximum value of 0.5. In this case, the maximum line voltage that is normalized based V_{DC} will be limited to $0.5\times\sqrt{3} \approx 0.86$. It is clear that 14% reduction in full DC utilization is a major disadvantage for this modulation technique.

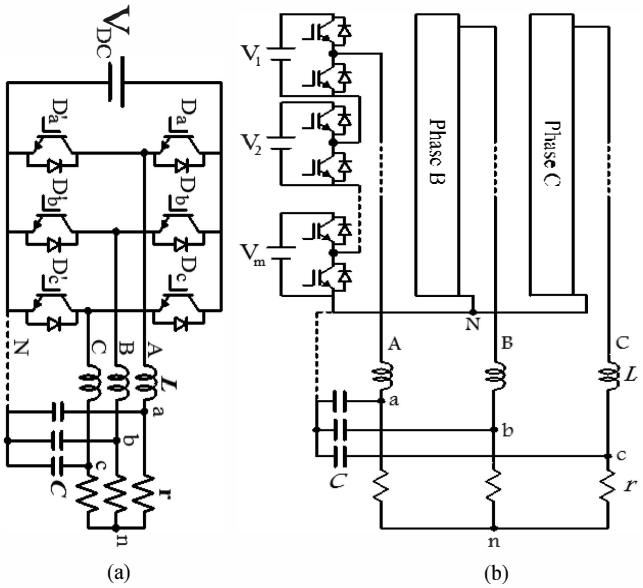


Figure 2. Differential connection of buck converters in three phases, (a) 2-level configuration, (b) multilevel configuration

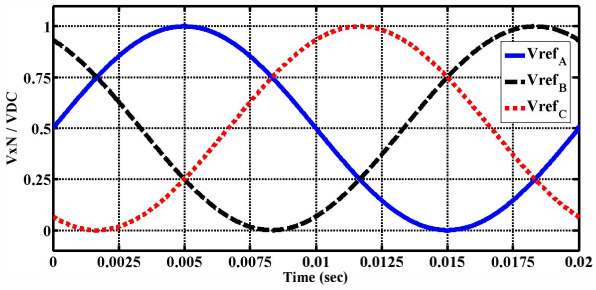


Figure 3. Three-phase duty cycles in Fix offset modulation by (3) at A=0.5

The dc utilization means the ratio of the output fundamental voltage to the dc link voltage (V_{DC}) [12].Three phase normalized voltage reference waveform according to (3) for maximum modulation index (A = 0.5) is shown in Fig. 3. As can be seen the waveforms have an equal fixed offset. These reference waveforms can be used for the discussed three phase differential multilevel converter with multi carrier base switching technique.

B. Applying third harmonic injection (THIPWM)

This method is used in order to increase the DC utilization in high modulation index. Instead of a sinusoidal reference a waveform with a fundamental and a third component is used [6]. Based on this modulation technique the required reference waveforms for the discussed differential converters are produced with (5). This waveforms for maximum modulation index (A=0.5) are shown in Fig. 4. Since the line voltage caused by difference between two phases voltage a DC offset as well as the third harmonic component will not be appeared on load voltages. With increasing of 15% in each phase's first component, full DC utilization will be obtained.

$$\begin{cases} V_{aN}/V_{DC} = D_a(t) = 1.15A\sin(\omega t) + 0.25A\sin(3\omega t) + A \\ V_{bN}/V_{DC} = D_b(t) = 1.15A\sin(\omega t + 2\pi/3) + 0.25A\sin(3\omega t) + A \\ V_{cN}/V_{DC} = D_c(t) = 1.15A\sin(\omega t - 2\pi/3) + 0.25A\sin(3\omega t) + A \\ 0 \le D(t) \le 1 \quad \Rightarrow \quad A \le 0.5 \end{cases} \tag{5}$$

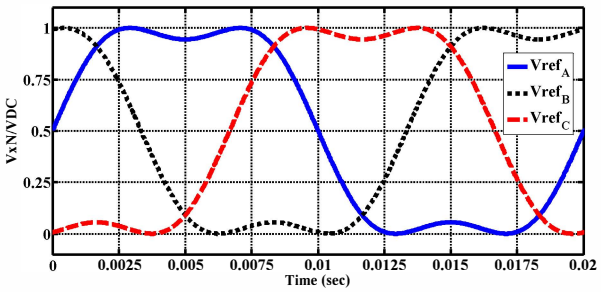
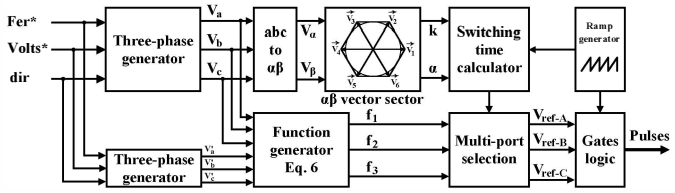
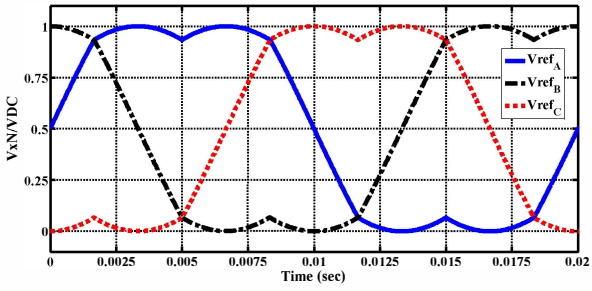


Figure 4. Duty cycles in the THIPWM according to (5) at A = 0.5



(a)



(b)

Figure 5. The SVPWM technique, (a) reference waveforms and gate pulses generating according to (6), (b) three-phase duty cycles for a full DC utilization.

C. Applying Space Vector PWM

Fig. 5(a) shows voltage reference waveforms generating for three phase differential converters with SVPWM method based on (6) [9]. Three phase normalized voltage reference waveforms for maximum modulation index are shown in Fig. 5(b). By using these waveforms as duty cycles in discussed multilevel converter full DC utilization will be obtained.

$$\begin{cases} f_1(t)= 0.14\times\max(V_a', V_b', V_c') + 0.86 \\ f_2(t)= -0.86\times(\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)) + 0.5 \\ f_3(t)= -0.14\times\max(V_a', V_b', V_c') + 0.14 \\ V_a = \sin(\omega t),\ V_b = \sin(\omega t + 2\pi/3),\ V_c = \sin(\omega t - 2\pi/3) \\ V_a' = \sin(2\omega t - 5\pi/6),\ V_b' = \sin(2\omega t - \pi/6),\ V_c' = \sin(2\omega t + \pi/2) \end{cases} \quad (6)$$

D. Applying offset optimization

Consider THIPWM method that with third harmonic injection can solve fix offset technique weakness and reach to full DC-link utilization. So for with switching losses reduction an efficient modulation technique will be available. The problem key is to find an optimized modulation with variable offset like THIPWM and SVPWM. So in (5) the common component $(0.25A\sin(3\omega t) + A)$ that shows a sinusoidal offset is replaced with an unknown time dependent $X(t)$ like (7). Equation (8) shows $X(t)$ will not be appeared at line voltages and A will be limited to 0.5. Summation of three first relationship at (7) results (9) that shows $X(t)$ is proportional to the sum of the three-phase duty ratios. With minimizing $X(t)$, the total switches ON time will be minimized. In this case, with 15% increasing in DC-link utilization, switching losses will be minimized.

$$\begin{cases} V_{aN}/V_{DC} = D_a(t) = 1.15A\sin(\omega t) + X(t) \\ V_{bN}/V_{DC} = D_b(t) = 1.15A\sin(\omega t + 2\pi/3) + X(t) \\ V_{cN}/V_{DC} = D_c(t) = 1.15A\sin(\omega t - 2\pi/3) + X(t) \end{cases} \quad (7)$$

$$\begin{cases} \dfrac{V_{ab}}{V_{DC}} = \dfrac{V_{aN} - V_{bN}}{V_{DC}} = D_a(t) - D_b(t) = 1.15A\sqrt{3}\sin(\omega t - \pi/6) \\ 0 \le D(t) \le 1 \quad \Rightarrow \quad 0 \le 1.15A\sqrt{3} \le 1 \quad \Rightarrow \quad 0 \le A \le 0.5 \end{cases} \quad (8)$$

Equation (9) shows $X(t)$ is proportional to the sum of three-phase voltages. Therefore, the objective function of the minimization problem can be set out as minimizing the sum of three phase voltages with respect to the DC negative pole N ($V_{aN}(t) + V_{bN}(t) + V_{cN}(t)$) with subjected to (10) for sinusoidal voltages production. Solving the optimization problem should be done for a number of points of the power frequency cycle f_p. If the total switching frequency that is sum of all levels switching frequency at the output voltage is considered f_s the required number of points in this case will be equal to f_s / f_p. The power frequency is 50Hz and the maximum considered switching frequency at LS-PWM is 3500Hz so the required point is 70. Optimization result by solving (7) with A=0.5 for full DC utilization is shown in Fig. 6. The outcome result is very interesting because switching operation is not required in One-third of the power cycle for each phase of differential multilevel converter.

$$X(t) = \frac{V_{aN} + V_{bN} + V_{cN}}{3\times V_{DC}} = \frac{D_a(t) + D_b(t) + D_c(t)}{3} \quad (9)$$

$$\begin{cases} (V_{aN}(t) - V_{bN}(t))/V_{DC} = 1.15A\sqrt{3}.\sin(\omega t - \pi/6) \\ (V_{bN}(t) - V_{cN}(t))/V_{DC} = 1.15A\sqrt{3}.\sin(\omega t + \pi/2) \\ V_{aN}(t),\ V_{bN}(t),\ V_{cN}(t) \ge 0 \\ 0 \le A \le 0.5 \end{cases} \quad (10)$$

IV. 16-Level Three-Phase Multilevel Converter

The discussed modulation techniques will be applied on a typical multilevel converter based on the converter shown in Fig. 2(b). This converter has been considered with four 2-level chopper with $V_1 = V_{dc}$, $V_2 = 2Vdc$, $V_3 = 4V_{dc}$, $V_4 = 8V_{dc}$ for the dc voltage sources in each phases. In this case, in accordance with switching states in table I, this converter will be able to produce 16 positive level at the output of each phase from 0 to 15 V_{dc} with stair of V_{dc}=5V. For example if the switches states of four stage at phase A are S_{a1}=1, S_{a2}=0, S_{a3}=1, S_{a4}=0 respectively, the output voltage V_{AN} is $V_{dc} + 4V_{dc} = 5V_{dc}$ =25V or with switches states S_{a1}=1, S_{a2}=1, S_{a3}=0, S_{a4}=1, V_{AN} is $V_{dc} + 2V_{dc} + 8V_{dc} = 11V_{dc}$ =55V. It is worth mentioning because of the connection of the negative output of the fourth module in all three phases to point N, the dc voltage source of this module in all three phases can be common but other modules require their own DC sources. So the total number of needed sources in this converter configuration will be ten. Other specification of 16-level differential converter are given in table II.

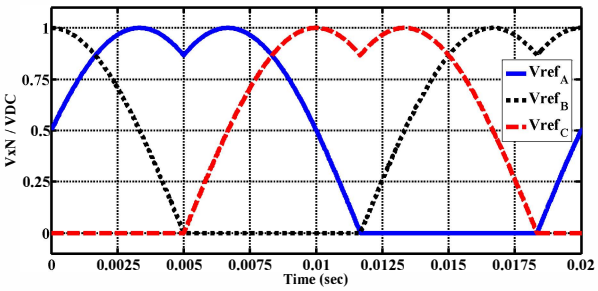


Figure 6. Calculated three-phase duty cycles by (9) at A=0.5 for optimized offset modulation technique.

A. Switching technique

Generally, the methods for determining the switching states with respect to a given reference waveforms can be divided to two fundamental frequency switching and high switching frequency techniques [14]. High frequency switching techniques are based on the comparison of a given reference waveform with high-frequency carriers with phase-shifted or level-shifted or a combination of level and phase shifted [14]. The gate signals production with LS-PWM technique for applying to the 16-level converter is shown in Fig. 7. By comparing the given reference waveform (U_{ref}) with 15 shifted-level carriers and summation of the comparators outputs a multilevel waveform between 0 to 15 will be produce that with applying to the switching states table(table I), the ON switches in each level will be obtained.

TABLE I. SWITCHING STATES FOR ONE PHASE OF THE 16-LEVEL CONVERTER

Switches states				V_{AN}/V_{dc}
S_{a1}	S_{a2}	S_{a3}	S_{a4}	
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
⋮	⋮	⋮	⋮	⋮
0	1	1	1	14
1	1	1	1	15

TABLE II. SPECIFICATION OF THREE PHASE 16-LEVEL CONVERTER

No	Title		Specifications	Quantity
1	Switches		IGBT	24
2	Switching technique		LS-PWM	---
3	Power supplies voltage	Half Bridge 1	$V_1=V_{dc}$=5V	3
		Half Bridge 2	$V_2=2V_{dc}$=10V	3
		Half Bridge 3	$V_3=4V_{dc}$=20V	3
		Half Bridge 4	$V_4=8V_{dc}$=40V	1
4	Load		r=15Ω	3
5	LC Filter Capacitor		L=20μF	3
6	LC Filter Inductance		C=2mH	3
7	LS-PWM Carrier freq		f_s=3500Hz	---
8	Fundamental frequency		f_p=50Hz	---

V. SIMULATION RESULTS

Simulation results using the Fix offset modulation with LS-PWM switching technique are shown in Fig. 8. This figure shows the three output voltages-to-N (V_{AN}, V_{BN}, V_{CN}), three output LC-filter-to-N (V_{aN}, V_{bN}, V_{cN}), three phase-to-neutral voltages and a line voltage (V_a, V_b, V_c, V_{ab}). Fig. 8(a) presents multilevel voltage waveforms with 16 levels at the dc output side of converter before LC-filter. Simulation results using the THIPWM modulation are shown in Fig. 9. As can be seen no dc stress nor third harmonic component appear at load voltages. With applying THIPWM full DC utilization can be achieved.

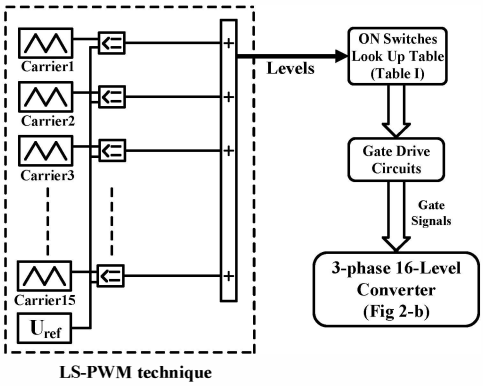


Figure 7. Gate signals generating with applying LS-PWM technique.

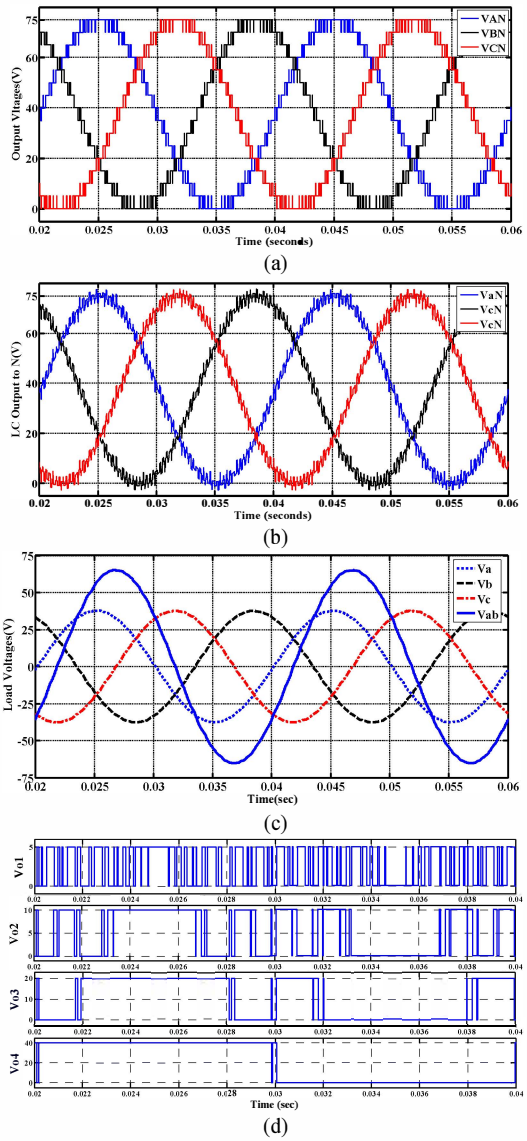


Figure 8. Simulation results by appling Fix offset modulation technique, (a) converter output voltages to N point, (b) load voltages to N point, (c) load voltages to neutral point (n), (d) output voltages of half bridges at phase A.

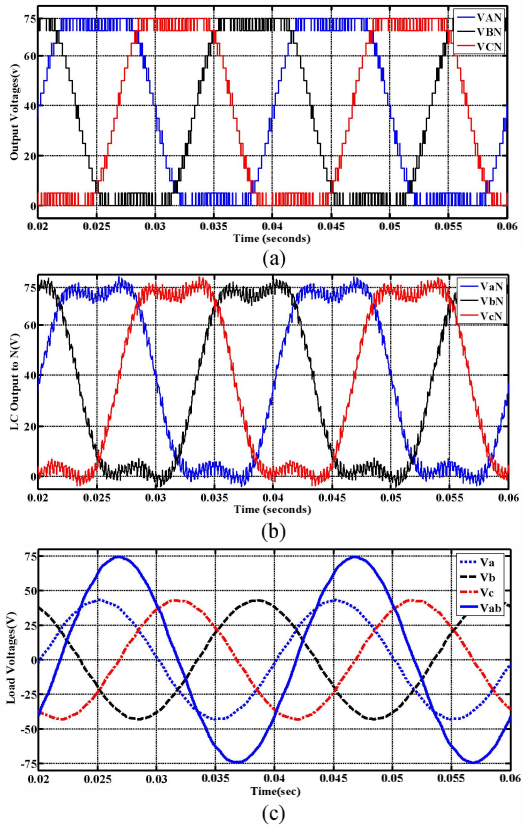


Figure 9. Simulation result by appling THIPWM modulation, (a) converter output voltages to N point, (b) load voltages to N point, (c) load voltages to neutral point (n).

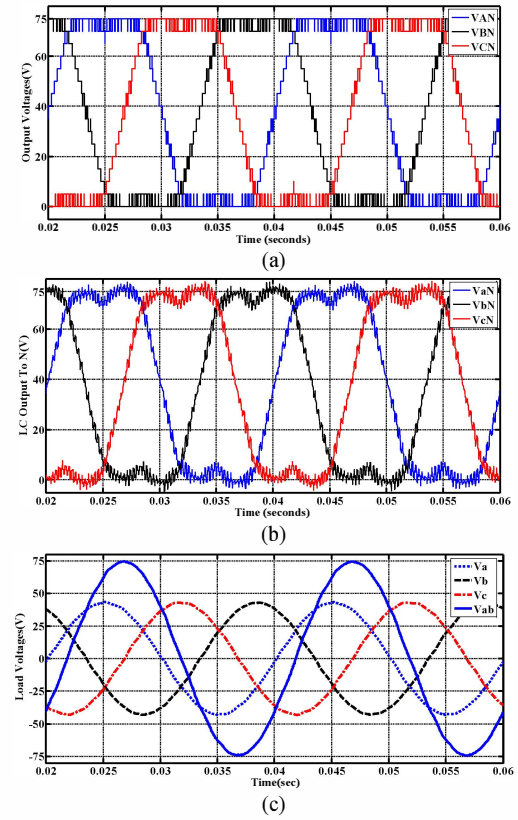


Figure 10. Simulation result by appling SVPWM modulation, (a) converter output voltages to N, (b) load voltages to N, (c) load voltages to neutral (n).

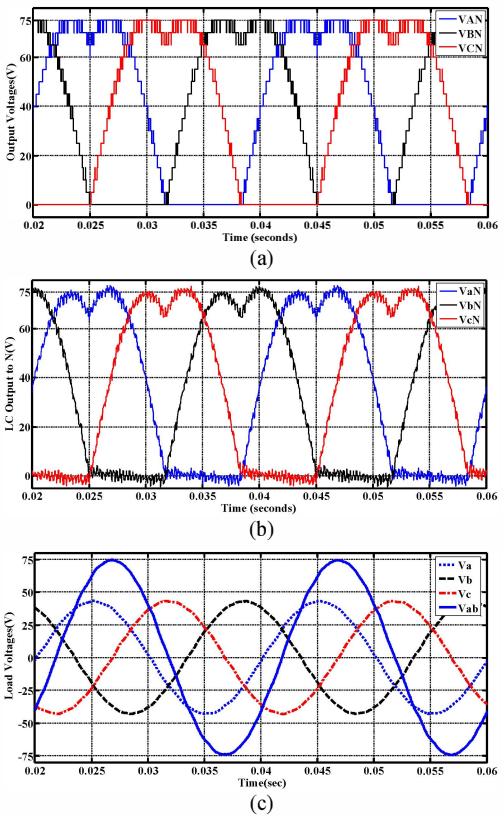


Figure 11. Simulation result by appling optimized offset modulation technique, (a) converter output voltages to N point, (b) load voltages to N point, (c) load voltages to neutral point (n).

In addition simulation results using the SVPWM modulation technique are shown in Fig. 10. Full DC utilization by using SVPWM modulation for 16-level three phase differential is available. Also as can be seen from simulation results in Fig. 11 with applying the optimized offset modulation full dc utilization has been achieved.

VI. Comparison of Discused Modulation Techniques

In order to better comparison, duty cycles of four discussed modulation technique are shown in Fig. 12. As it can be seen duty cycle of SVPWM and THIPWM are very similar to each other while the optimized offset has an asymmetry duty cycle waveform with one third off at total duty cycle time. So the switching losses of optimized offset modulation is 33% lower than other three methods. In addition the offset waveforms of four reviewed modulation techniques are shown in Fig. 13. As it can be seen except of Fix offset other modulation techniques has time variable offset. Also SVPWM and THIPWM has similar offset with average value equal to Fix offset but the optimized offset has a different offset waveform with lower average value.

The RMS value and THD of converter output line voltage (V_{AB}) with applying four modulation technique at different modulation index are given in table III. With increasing modulation index (M_a) because of the number of output voltage levels increase, more sinusoidal waveform with lower THD will be achieved. For example at M_a=0.33 the converter output voltages are multilevel waveforms with only six levels while for M_a=0.86 there are fourteen levels with more better THD. As it

can been from table III the optimized offset modulation technique has the highest RMS value with the lowest THD at different modulation indexes.

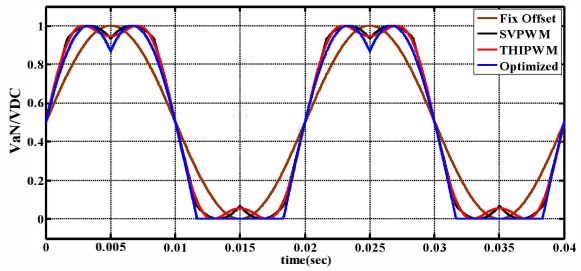


Figure 12. Duty cycles of four discussed modulation techniques.

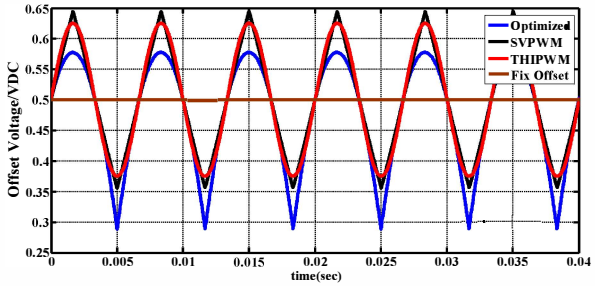


Figure 13. Simulated normalized offsets by appling four modulation techniques.

TABLE III. LINE VOLTAGES THD AND RMS VALUE BY APPLING FOUR DISCUSSED MODULATION TECHNIQUES

Modulation technique	Parameters	Modulation Index				
		0.33	*0.5*	*0.75*	*0.86*	*1*
Fix offset	THD (%)	13.2	9.1	6	5	4.4
	Vrms (V)	15.3	23.7	34.5	39.5	46
SVPWM	THD (%)	11.4	7.8	5	4.5	3.7
	Vrms (V)	17.6	26.6	39.9	45.6	53
THIPWM	THD (%)	11.6	7.9	5	4.4	3.6
	Vrms (V)	17.1	26.3	39.8	45	52.3
Optimized Offset	THD (%)	11.4	7.7	4.9	4.3	3.4
	Vrms (V)	17.8	26.7	40	45.8	53.2

VII. CONCLUSION

This paper analyzes the three-phase differential multilevel converters based on three separate multilevel buck-converters. It is shown that DC offset has a special importance in modulation techniques. Assuming this parameter variable instead of a fixed one and optimizing it with some constraints, it can be found a new efficient modulation technique. The proposed optimized variable modulation technique is applicable for three-phase differential converters including multilevel ones. For a comprehensive comparison between similar modulation techniques, optimized offset with Fix offset, THIPWM and SVPWM have been applied on a three-phase 16-level converter. The results show the proposed modulation is an optimized and efficient technique. The optimized offset modulation technique has major advantages like; full DC utilization, lower switching losses, higher efficiency and simplicity in implementation.

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, "Recent Advances and Industrial Applications of Multilevel Converters" IEEE Trans. Ind. Electron, vol. 57, no. 8, Agu. 2010, pp.2553-2580.

[2] R. Teichmann, M. Malinowski, S. Bernet, "Evaluation of three level rectifiers for low-voltage utility applications", IEEE Trans. Ind. Electron, vol. 52, no. 2, 2005, pp. 471–481.

[3] J. Rodriguez, J.S. Lai, F.Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications", IEEE Trans. Ind. Electron, vol. 49, no, 4, 2002, pp. 724–738.

[4] B. Eskandari, M.T. Bina, "Support vector regression-based distortion compensator for three-phase DC–AC boost-inverters: analysis and experiments", IET Power Electronic, vol. 7, no. 2, 2014, pp. 251 - 258.

[5] B. Eskandari, M.T. Bina, M.A. Golkar, "New concept on sinusoidal modulation for three-phase DC/AC converters: analysis and experiments" , IET Power Electronic, vol. 7, no. 2, 2014, pp. 357 - 365.

[6] B. Urmila, D. Subbarayudu, "Multilevel Inverters: A Comparative Study of Pulse Width Modulation Techniques" International Journal of Scientific & Engineering Research, vol. 1, no. 3, 2010, pp. 1-5.

[7] S.K. Chattopadhyay, C. Chakraborty, B.C. Pal, "A hybrid multilevel inverter topology with third harmonic injection for grid connected photovoltaic central inverters" IEEE International Symposium on Industrial Electronics (ISIE), 2012, pp. 1736 - 1741.

[8] V.N.B. Reddy, C.S. Babu, S.N. Raq, "Comparison of Modulation Techniques for Multilevel Inverter fed Permanent Magnet Synchronous Motor" International Journal of Engineering Science and Technology, vol. 2, no. 10, 2010, pp.5206-5214.

[9] R.S. Kanchan, M.R. Baiju, K.K. Mohapatra, P.P. Ouseph and K. Gopakumar, "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages", IET Electric Power Application, vol. 152, no. 2, 2005, pp. 297 – 309.

[10] B. P. McGrath, D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters", IEEE Trans. Ind. Electron., vol. 49, no. 4, 2002, pp. 858–867.

[11] Y. Liu, F.L. Luo, "Trinary hybrid 81-level multilevel inverter for motor drive with zero common-mode voltage", IEEE Trans. Ind. Electron., vol. 55, no.3, 2008, pp. 1014–1021

[12] Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, "Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter" IEEE Trans. Power Electron., vol. 24, no. 1, 2009, pp. 25–33.

[13] V.T. Somasekhar, B.V. Reddy. ; K. Sivakumar, "a four-level inversion scheme for a 6 n-pole open-end winding induction motor drive for an improved DC-Link utilization" IEEE Trans. Ind. Electron., vol. 61, no. 9, 2014, pp. 4565 - 4572.

[14] I. Colak, E. Kabalci. E, R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes", J. Energy Convers. Manage., vol. 52, no. 2, 2011, pp. 1114–1128.