

A Combined DC-Filter and Optimized Modulation to Absorb DC-Link Oscillations of Cascaded H-Bridge Converters

M. Tavakoli Bina¹, B. Eskandari²

¹ Associate Professor, Faculty of Electrical Engineering, K. N. Toosi University of Technology, tavakoli@kntu.ac.ir

² M.Sc. Student, Electrical Engineering, Faculty of Electrical Engineering, K. N. Toosi University of Technology, b_eskandari@kntu.ac.ir

Abstract: Cascaded H-bridge converters may well be used for applications requiring higher voltages, without needing series connection of semiconductor switches. Two problems are necessary to be addressed; first, the AC voltages of the sub-modules of the cascaded converter which are unequal due to the deployed modulation technique, thus introducing different fundamental components and harmonic contents. Second, is the DC-links of sub-modules that are subjected to low-frequency oscillations when operating under three-phase unbalance condition and/or single-phase active power exchange. This paper begins with the first problem, suggesting a generalized swapping technique for a cascaded H-bridge converter. This is applied to the SPWM and the optimal PWM, while the optimal PWM is suggested to be subjected to a complementary constraint. A five-level H-bridge cascaded converter is developed to implement the suggested modulations. Practical results confirm that AC voltages of the sub-modules are equalized. Furthermore, three various external DC active filter circuits are presented to tackle the second problem, including the independent DC source, the auxiliary S-bridge and the buck-boost design. These circuits are simulated, and their performances are compared. Moreover, the buck-boost design is implemented, and applied to the DC output of a single-phase full-bridge rectifier. Then, three control strategies are further tested on the buck-boost compensating circuit. Experimental results show that the effective value of the DC ripples is considerably lowered down in comparison with the original DC oscillation.

Keywords: Cascaded converter, DC-link oscillation, balanced AC voltages, optimal-PWM, SPWM.

چکیده: مبدل‌های چند سطحی کاسکاد در کاربردهایی که ولتاژ بالا نیاز است مورد توجه قرار گرفته اند. در حالیکه این امر از سری کردن سوییچ‌های نیمه هادی جلوگیری می نماید، دو مساله مهم نیز در اینگونه مبدل‌ها باید مورد مطالعه واقع گردند. اول، مساله توزیع متعادل ولتاژ AC در خروجی هر یک از مبدل‌های سری شده که می‌توانند در اثر مدولاسیون بکار گرفته شده بوجود آیند. دوم، مساله تعادل ولتاژهای لینک DC که در اثر عدم تعادل لینک AC و یا تبادل توان اکتیو حاصل میگردد. این مقاله با مساله اول شروع کرده و روش جابجایی عمومی برای مبدل‌های کاسکاد نوع H ارائه مینماید. ضمن در نظر گرفتن مدولاسیون SPWM و PWM بهینه، یک مبدل پنج سطحی ساخته شده و روش ارائه شده توسط میکروکنترلر برنامه ریزی گردیده است. نتایج عملی بدست آمده یکسان سازی خروجی AC مبدل‌های نوع H را تایید مینماید. بعلاوه، سه روش اکتیو جهت فیلتر کردن نوسانات سمت DC ارائه شده است. همچنین، یک مبدل باک - بوست نیز به همراه سه روش کنترلی پیشنهاد و پیاده سازی شده است که نتایج عملی موید کاهش چشمگیر ریبیل سمت DC نسبت به نوسانات اولیه آن می باشد.

کلمات کلیدی: مبدل کاسکاد، نوسانات سمت DC، متعادل‌سازی خروجی‌های AC، PWM، بهینه، SPWM

Nomenclatures:

N : total number of H-bridges
 K : number of switching instants

α_{ij} : the j th switching instant of the i th H-bridge converter

V_{a-n} : the n th harmonic component
 d : practical duration between two consecutive switching instants
 V_{dc} : the DC voltage of the compensating H-bridge converter
 t_{on} : the on-time duration of each switch
 V_f : oscillations on top of the DC-link
 C_{f1} and C_{f2} : DC-link active filter capacitances
 C : DC-link capacitance
 ΔV : hysteresis-like positive band
 L : AC-side commutation inductance
 V_L : the voltage drop on the inductance L
 i_L : current through the inductance L

1- Introduction

Multilevel converters can potentially overcome the practical impediments associated with the series connection of semiconductor switches to increase the system voltage [1]-[4]. Figure 1(a) shows a five-level cascaded H-bridge converter with which the harmonic performance is expected to be improved, while the supply voltage is distributed across the sub-modules. However, two problems should be considered. First, the applied voltage can be distributed unevenly across the H-bridge converters depending on the applied modulation technique. Second, the AC voltages of the sub-module may also add different harmonic contents, both in magnitude and phase. Since the series current is identical for all converters, sub-modules could be subjected to different power levels. Thus, it is also expected to observe unbalance of the DC-link voltages as well as oscillation on each DC-link voltage.

Second, each H-bridge sub-module exchanges *instantaneous* active power with the electrical network and thereby leading to DC-link voltage oscillations. (Note that the *average* absorbed active power by the converters in a power system period could be still as low as the power losses of the converters.) This exchanged power will highly affect the DC-link voltage of an H-bridge converter, causing low frequency oscillations (e.g. 100/120 Hz oscillations for synchronous frequency 50/60 Hz like that shown in Fig. 1(c)). The bigger the exchanged power within the sub-module, the larger will be the observed oscillations on top of the DC-link voltage [5]-[6].

Conventional PWM techniques have been introduced in related literatures. These techniques are simple to implement, while the two raised problems will, more or less, persist in the H-bridge sub-

modules. Since harmonic magnitudes of the H-bridge converters may vary, different oscillating components with different magnitudes can be added to the DC-link voltages. Some other techniques objectively eliminate certain harmonics. E.g., an optimized pulse width modulation technique (OPWM) is presented in [7] wherein the modulation is capable of eliminating any given number of harmonics. The problem, however, is that some optimized switch-on or switch-off durations might be very short. In practice, the switching frequency of power semiconductor switches is limited. Hence, implementation of the resulting optimized modulation cannot be fully achieved.

This paper begins with sinusoidal PWM (SPWM) and the OPWM techniques for cascaded H-bridge converters in order to address the first problem of uneven AC voltage distribution. One suggestion is introduced to improve the conventional SPWM for five-level cascaded H-bridge converters. This will make AC voltages of the two sub-modules similar, while the DC-link oscillations are still there. A five-level cascaded H-bridge converter is implemented to verify above suggestion. Furthermore, the constraints of the OPWM are so improved that the switching durations can actually be programmed. Then, the improved OPWM is also verified by the five-level converter, and practical results are compared with those of the improved SPWM. To deal with the DC-link oscillations, three different DC-filters are proposed to be connected across the DC-link capacitor, including the independent DC source, auxiliary S-bridge converter and the buck-boost compensating converter. The suggested methods are then examined and simulated by MATLAB to assess their performances and their suitability for the cascaded H-bridge converters. Among these converters, the buck-boost design is implemented, and applied to a single-phase full-bridge rectifier in which the DC oscillations are strongly imposed by the DC source. Practical results confirm that this latter proposal introduces marked improvement in lowering effective values of the DC-link oscillations.

2- Generalized switching pulse transition

Consider the cascaded five-level converter in Fig. 1(a) which is modulated through a conventional SPWM. MATLAB simulations are so arranged that four triangular carriers of 2100 Hz (twice as the number of H-bridges) are compared with a sinusoidal reference (50 Hz). Resultant comparisons lead to the output waveforms shown by Fig. 1(b) including two AC voltages of the H-bridges together with the total

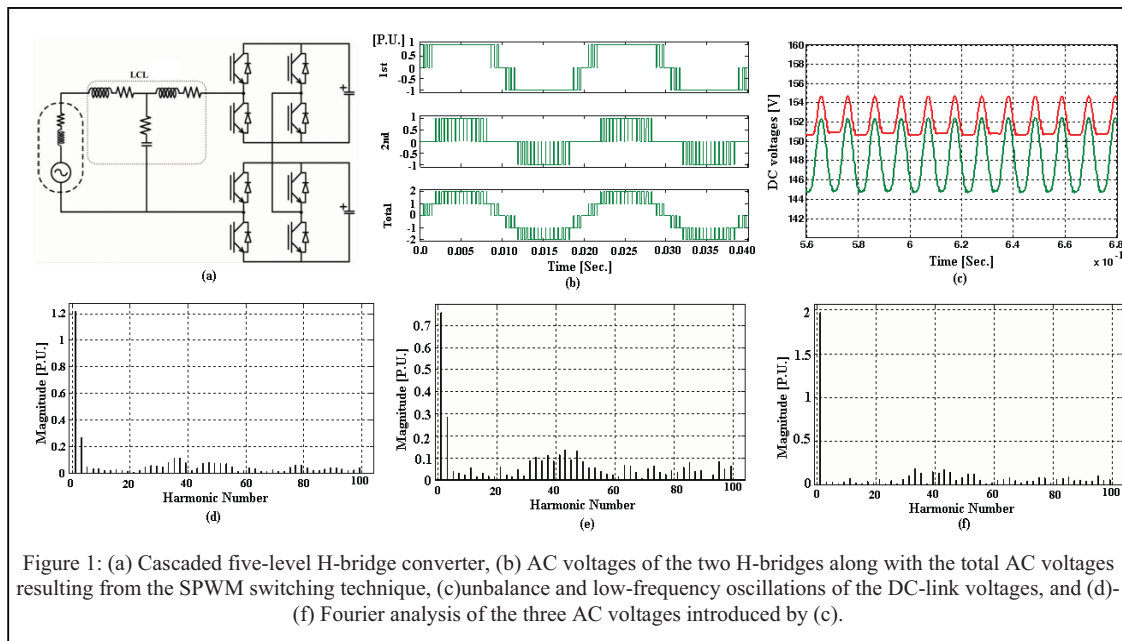


Figure 1: (a) Cascaded five-level H-bridge converter, (b) AC voltages of the two H-bridges along with the total AC voltages resulting from the SPWM switching technique, (c) unbalance and low-frequency oscillations of the DC-link voltages, and (d)-(f) Fourier analysis of the three AC voltages introduced by (c).

cascaded voltage. Fourier analysis of these waveforms is introduced in Figs. 1(d)-(f). The analysis shows that the first H-bridge introduces a fundamental component of 1.215 P.U., the second H-bridge 0.755 P.U., and the total cascaded voltage 1.972 P.U. This clearly implies that the first H-bridge has a bigger modulation index, and higher duty ratios in comparison with the second converter. Since the series current is identical for both converters, the DC-link voltage of the first H-bridge is different from the second one. Hence, the first H-bridge converter introduces larger oscillations compared to the second one and this is due to their different power levels. Simulations shown by Figs. 1 confirm the presence of the two stated problems (uneven AC voltage distribution and DC-link oscillation).

2.1 Switching pulse transposition (SPT)

The conventional SPWM not only produces unequal fundamentals, but it also produces different harmonic levels for the two H-bridges. One suggestion for symmetrical operation of the sub-modules could be a *regular transposition* of the switching pulses that are generated by the conventional SPWM. In practice, the SPT should be performed within every synchronous period such that a DC component *will not* appear on the AC voltage of a sub-module. For instance, when the switching pulses of the two sub-modules (generated by the conventional SPWM) are swapped over every half of a synchronous period, simulations show nonzero DC values on AC voltages of both H-bridge converters.

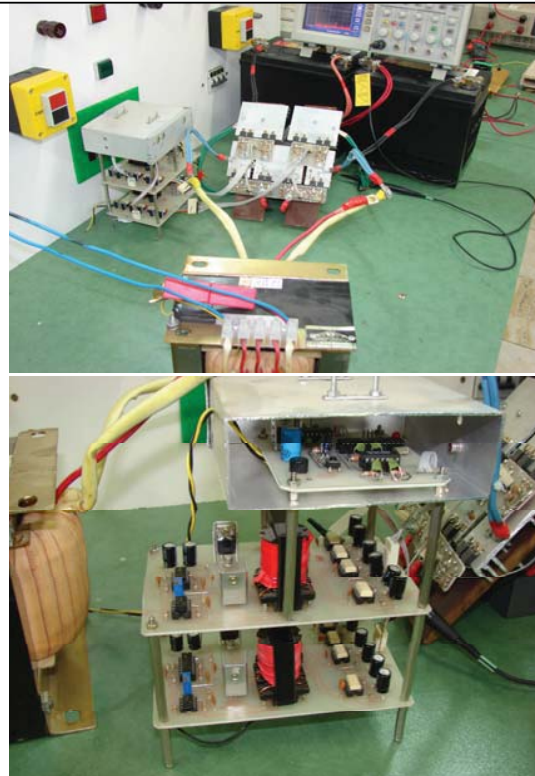


Figure 2: Experimental arrangement for balancing the capacitor voltages using the improved SPWM and the OPWM techniques.

As the number of H-bridges increases, application of the SPT among the sub-modules needs to be regulated.

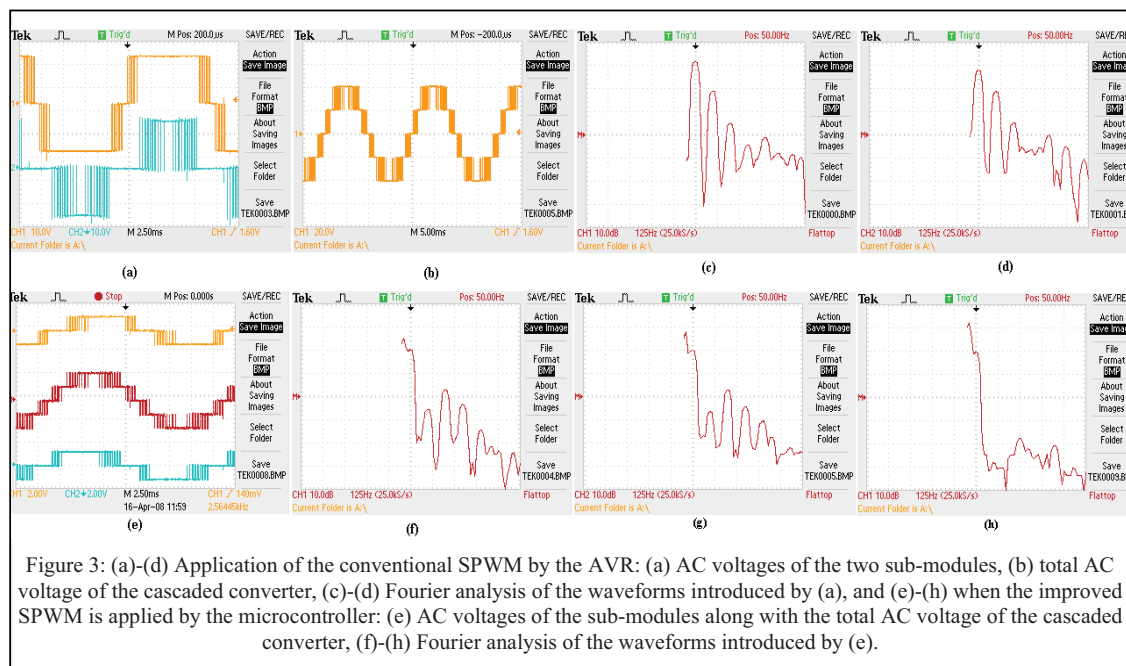


Figure 3: (a)-(d) Application of the conventional SPWM by the AVR: (a) AC voltages of the two sub-modules, (b) total AC voltage of the cascaded converter, (c)-(d) Fourier analysis of the waveforms introduced by (a), and (e)-(h) when the improved SPWM is applied by the microcontroller: (e) AC voltages of the sub-modules along with the total AC voltage of the cascaded converter, (f)-(h) Fourier analysis of the waveforms introduced by (e).

Figure 4 illustrates how 30 SPT occur during a half-cycle among five H-modules ($H_1 \sim H_5$). Every SPWM outcome is applied first to H_1 during $[0^\circ, 6^\circ]$, the second is transmitted to H_2 during $[6^\circ, 12^\circ]$, third to H_3 during $[12^\circ, 18^\circ]$, fourth to H_4 during $[18^\circ,$

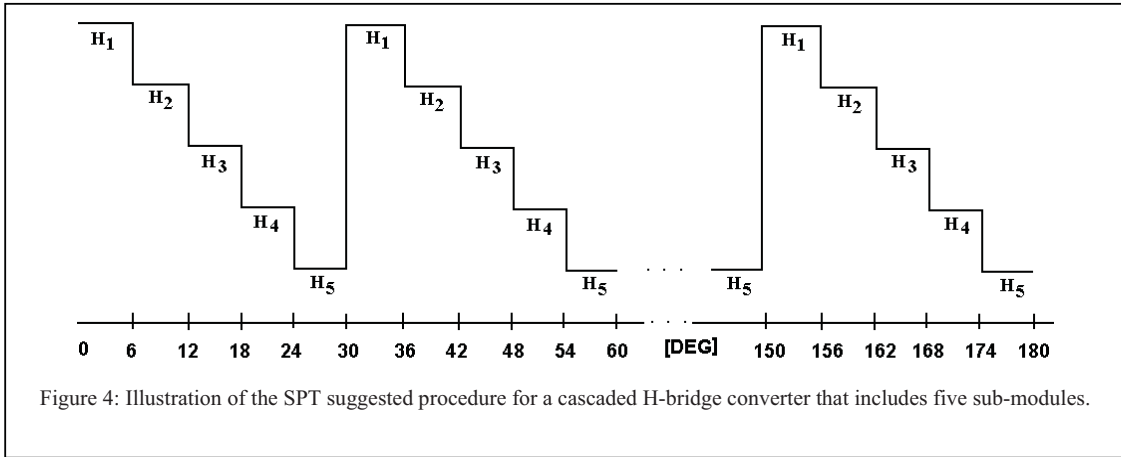


Figure 4: Illustration of the SPT suggested procedure for a cascaded H-bridge converter that includes five sub-modules.

modules nearly equally. According to these recorded results, the number of swapping of the switching pulses within every half-cycle equals to six times of that of the number of the sub-modules (e.g. 12 SPT for two sub-modules and 30 SPT for five sub-modules). The only exception is that of the two sub-module in which the swapping can also take place every quarter of a synchronous period in addition to the suggested general rule (transposition of the SPWM outcome every 15°). Simulations confirm that the harmonic behavior of both sub-modules are quite similar, in particular, both fundamentals and low order harmonics become identical.

24°] and fifth to H_5 during $[24^\circ, 30^\circ]$. Then, this procedure is repeated six times until the half cycle is completed. It is noticeable that various repeating procedures may be deployed for the six SPT amongst the sub-modules. Nevertheless, the best solution is achieved when the repeating procedure always starts from the first sub-module down to the last one as is shown in Fig. 4.

2.2 Experimental validation

A five-level cascaded H-bridge converter, shown by Fig. 1(a), is implemented to examine the equalization of the AC voltages of the sub-modules. Figures 2(a)-(b) show the power circuit together with

the microcontroller and switching driver circuits. Sixteen switches (MOSFET 2N06L05) are used in all, eight for each sub-module, where every two parallel switches make one pack. The IC number TLP250 is used for switching drive circuits that transmit the switching pulse train produced by the AVR microcontroller. The microcontroller consists of two ATMEGA8-16PU units. A 15 Amp fast fuse is used to protect the device. Two 12 V batteries supply the DC-link voltage, and a 1200 VA transformer is optionally available to be connected either to 220 V loads or to a possible grid connection (synchronization techniques have to be applied).

TABLE I: THE SUGGESTED PST FOR THE SPWM IN ORDER TO MAKE FUNDAMENTALS AND HARMONIC CONTENTS NEARLY THE SAME.

Number of cascaded H-bridges	Duration of one transposition in Degrees	Number of repeating of transpositions during each half-cycle	Total number of transpositions each half cycle
2	15°	6	12
3	10°	6	18
4	7.5°	6	24
5	6°	6	30
6	5°	6	36

Both the conventional SPWM and the suggested complementary improvement to the conventional SPWM have been programmed using the AVR microcontroller, and applied to the cascaded five-level converter. Four triangular carrier frequencies are all 2100 Hz. Experimental results are shown in Figs. 3(a)-(d) for the conventional SPWM, and Figs. 3(e)-(h) for the improved SPWM. Figures 3(a) and 3(e) demonstrate the AC voltages of the two sub-modules, and Figs. 3(b) and 3(f) show the total AC voltage of the five-level cascaded converter. To find out the effect of switching pulse swapping in every quarter, Fourier analysis of the two modulating programs are compared. Figures 3(c)-(d) zoom in the fundamentals as well as the low order harmonics of the two H-bridge AC voltages for the conventional SPWM. While the difference between the fundamentals is about 4dB (their ratio is about 1.58 like the simulations of Fig. 1), the harmonics also show different magnitudes. Considering the improved SPWM, Figs. 3(g)-(h) verify that both fundamentals are nearly identical, and the harmonic behavior of sub-modules are quite similar. It should be noted that low-frequency oscillations of the DC-links still remain as an issue for both conventional

SPWM and the improved one. This is even worse in the case of the improved SPWM compared to the conventional SPWM simulated by Fig. 1(c).

3- Simulation Results

Conventional multilevel SPWM schemes produce uneven fundamental voltages for the H-bridge sub-modules [14]-[18]. As an alternate technique, optimized algorithms are introduced in [6]-[10], to eliminate certain harmonic components by seeking the best switching instants. Assume N H-bridge converters are cascaded wherein every sub-module's AC voltage has both half-wave and quarter-wave symmetry. Then, determination of switching instants during each quarter-period is enough to recognize the whole period, and the Fourier series include only odd sinusoidal terms ($\sin(n\omega t)$). Hence, general description of the n th harmonic voltage using the Fourier series for N cascaded H-bridges and K switching instants within each quarter-wave is calculated as below:

$$V_{a-n} = \frac{4}{n\pi} \sum_{i=1}^N \sum_{j=1}^K (-1)^{k+1} \cos(n\alpha_{ij}) \quad (1)$$

Where the angle α_{ij} is the j th switching instant of the i th H-bridge converter, and V_{a-n} is the n th harmonic component of the total cascaded converter voltage. It is shown in [7] that harmonics up to the order $(2NK-1)$ should be eliminated for N sub-modules and K switching instants. An optimization problem can now be arranged having an objective function that minimizes the remaining odd harmonics starting from the third up to $(2NK-1)$. This is also subjected to several constraints. One necessary condition has to be satisfied by all sub-modules AC voltages on having identical fundamental magnitudes equal to $\frac{|V_{a-1}|}{N}$. This constraint introduces N equations, each having K unknown switching instants. Also, obvious conditions have to be set on K ascending angles α_{ij}

for each sub-module within the period of $\left[0, \frac{\pi}{2}\right]$. In

practice, a certain value should be considered between every two consecutive switching instants (d) to guarantee proper switching transitions. Thus, the third group of limitations is proposed here (added in (2)) in which the *pulse widths are bigger than a certain value d* (e.g. 10 μ s) for implementation purposes. Choosing this value depends on the switch

technical specifications, including the turn-on and turn-off durations that affect the switching frequency. The combinatorial optimization problem

Table II lists a typical lookup table containing the obtained optimal switching instants for $N=2$ and $K=21$ according to the stated procedure when

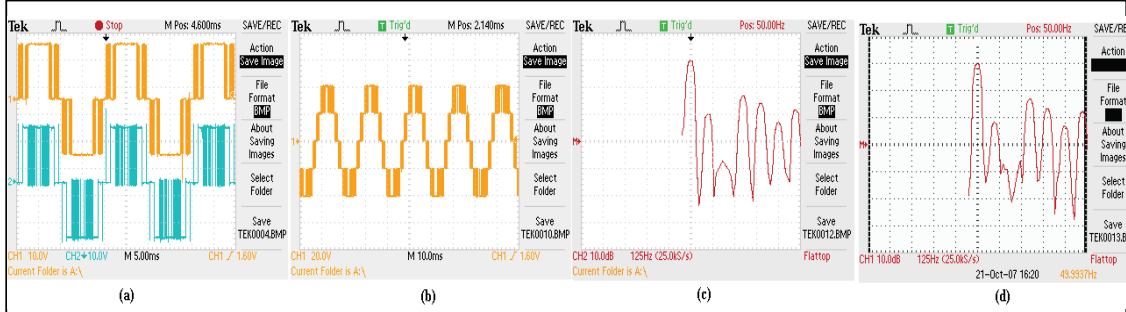


Figure 5: Application of the complementary optimal switching modulation by the AVR: (a) AC voltages of the two sub-modules, (b) total AC voltage of the cascaded converter, (c)-(d) Fourier analysis of the waveforms introduced by (a).

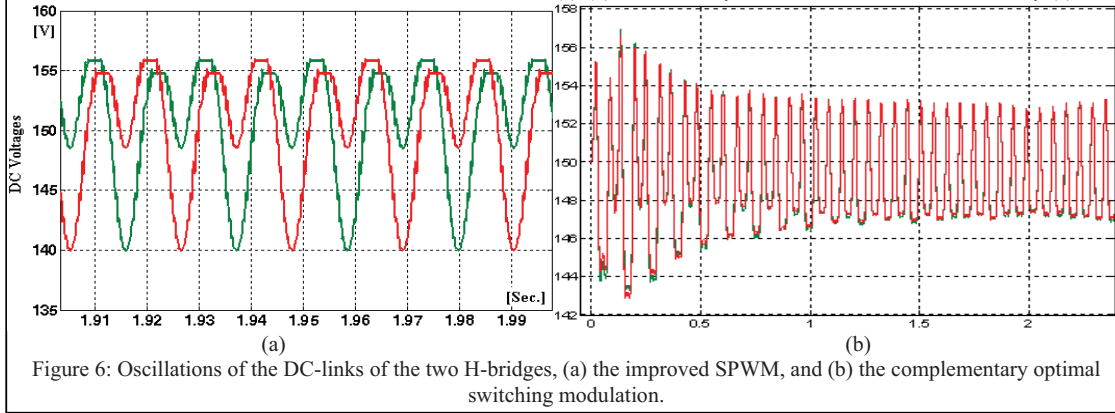


Figure 6: Oscillations of the DC-links of the two H-bridges, (a) the improved SPWM, and (b) the complementary optimal switching modulation.

can be formed as below:

$$\begin{aligned} & \text{Minimize } \sum_{\substack{n=3 \\ n \text{ is odd}}}^{2NK-1} V_{a-n}^2 \\ & \text{Subject to: } \begin{cases} \frac{4}{\pi} \sum_{j=1}^K (-1)^{k+1} \cos(\alpha_j) = \frac{|V_{a-1}|}{N} \\ 0 < a_{i1} < a_{i2} < \dots < a_{iK} < \frac{\pi}{2} \\ a_{i2} - a_{i1} \geq d \\ a_{i3} - a_{i2} \geq d \\ \vdots \\ a_{iK} - a_{i(K-1)} \geq d \end{cases} \quad \text{for } i = 1, 2, \dots, N \end{aligned} \quad (2)$$

3.1 Implementation of the complementary optimal modulation

The complementary optimal modulation of (2) can be solved using genetic algorithm. Since different initial conditions lead to different local minimums, ninety different initial conditions within $[0^\circ, 90^\circ]$ are applied to the optimization problem. Solutions are sorted according to their resultant THD%. The solution with the lowest THD% is selected and stored in a lookup table by the microcontroller. This process is repeated for various fundamental magnitudes, which eventually provides all the needed lookup tables for the microcontroller.

$d=10\mu\text{s}$ and $|V_{a-1}| = 36 \text{ dB}$ (about 63 V). Switching angles, related to other three quarters of the waveform, can simply be generated according to the assumed quarter-wave and half-wave symmetry for the waveform.

TABLE II: THE COMPLEMENTARY OPTIMAL SOLUTION LISTING THE SWITCHING INSTANTS OF THE FIRST QUARTER OF THE WAVEFORM THAT IS STORED AS A LOOKUP TABLE.

Sub-module Number	Optimized switching instants in the first quarter-period (angles in degrees)									
1	12	13	15	17	25	27	28	30	31	32
Cont. 1	36	41	43	45	46	48	50	58	59	64
2	8	9	19	21	22	25	28	29	31	36
Cont. 2	40	45	46	52	53	55	56	61	62	76

The microcontroller is then uploaded with all the obtained optimal solutions, and the modulation program is applied to the five-level cascaded H-bridge converter. Figure 4 shows the implementation outcomes. Both AC voltages of the two H-bridges are shown in Fig. 4(a), and the total cascaded voltage in Fig. 4(b). Comparing the fundamentals of the two sub-modules, it can be seen that they are slightly

different (29.8 dB and 30.14 dB). Hence, the switching pulses are *swapped* every *quarter-period*, and applied to the sub-modules. Figures 4(c) and 4(d) illustrate the Fourier analysis of the two AC voltages of the sub-modules, showing identical fundamentals for them with similar low-order harmonic behaviours.

Practical results indicate that both the complementary optimal switching modulation and the improved SPWM are capable of distributing identical fundamental AC voltages on the two sub-modules. However, the complementary optimal modulation with quarter-period swapping provides *better* AC voltage distribution and harmonic behaviour compared to the improved SPWM. But, both methods are still unable to attenuate the DC-links oscillation sufficiently as shown by simulations in Figs. 5(a)-(b). While the steady state peak-to-peak oscillation magnitude is below 16 V for the improved SPWM in Fig. 5(a), it is less than 7 V for the complementary optimal modulation in Fig. 5(b).

4- Suppression of DC-link oscillations

Connection of various DC passive/active filtering circuits across the DC capacitor is discussed in [11]. Predominant frequency of these oscillations is related to the second harmonic when the power system operates at 50/60 Hz. Other higher harmonic orders can also be present if the applied voltage includes any components in addition to the synchronous frequency. Typical uncompensated DC-link oscillations are shown in Figs. 5(a)-(b) when the improved SPWM and the OPWM modulation techniques are used, respectively. A PI controller is used to control the phase angle of the H-bridges output voltages such that the average DC-voltage remains fixed at 150 V.

One approach to filter out the low-frequency oscillations of the DC-links may be a passive LC-filter tuned at 100/120 Hz. This would effectively reduce oscillations. Nevertheless, the disadvantages of the passive LC-filters are their high cost, big parameters and size. Hence, the following subsections suggest and examine new designs that make use of active filters to damp the oscillations effectively.

4.1 Independent DC source (IDC): Proposition 1

The proposition of Fig. 6(a) uses the idea of passive LC-filter to absorb the oscillations in which the inductance of the passive filter is replaced by the primary winding of a transformer. The secondary of

the transformer is connected to a low-power low-voltage H-bridge converter through a passive low-pass LCL-filter. The suggested design provides much more satisfactory attenuation of DC-link oscillations compared to the passive LC-filter. Thus, the control and operation of this proposal will be examined in detail.

First, the oscillations of DC-link voltage (V_f) is extracted by subtracting the average value from the exact value of the DC-link voltage. Using the zero-order hold (ZOH) function of SIMULINK, the sampled signals (rated at 10 kHz) are converted to continuous signals. Then, the volt-second balance law is applied to each switching period ($100 \mu s$) to find the duty ratio of each switch as follows:

$$V_{dc} \times t_{on} = V_f \times 100(\mu s) \quad (3)$$

Where V_{dc} is the DC voltage of the compensating H-bridge converter, and t_{on} is the on-time duration of each switch. Computing t_{on} of the switches, they are applied to the compensating H-bridge converter. The whole design is simulated with MATLAB, where the transformer has a turn ratio slightly bigger than one. Figure 6(c) shows the compensated DC-link oscillations, which is largely attenuated down to about 2.5 V peak-to-peaks (or 1.67%).

It is noticeable that the compensating elements including the DC source, transformer, low-pass filter and switches operate under low-voltage low-power conditions. But in practice, according to (3) the lower the magnitudes of oscillations (V_f), the lower the duty ratios of switches will be. This implies a limit on reduction of magnitudes of oscillations as a drawback of the method. To remedy this, the voltage V_{dc} can be decreased when the oscillations are needed to be attenuated significantly. This also will add extra-cost to the converter for developing regulated controllable V_{dc} .

4.2 Auxiliary S-bridge compensation (ASC): proposition 2

This proposal uses two identical capacitors (C_{f1} and C_{f2}) along with three switches for each DC-link like that which it is illustrated in Fig. 6(b). Capacitances C_{f1} and C_{f2} have identical average DC voltages equal to three quarters of the DC-link voltage of capacitor C . Three switches are operated in a way that when the DC-link voltage is increased beyond a positive band (ΔV), the two vertical switches are turned on and the horizontal switch turns off. This puts both capacitances C_{f1} and C_{f2} in parallel, absorbing charging currents through the inductance L from C by the following slope:

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{V_{DC} - \frac{3}{4}V_{DC}}{L} = \frac{V_{DC}}{4L} \quad (4)$$

other drawbacks are the design costs, large size and occupying space. Hence, another suggestion is raised in which a buck-boost circuit is responsible for transferring energy between the DC-link

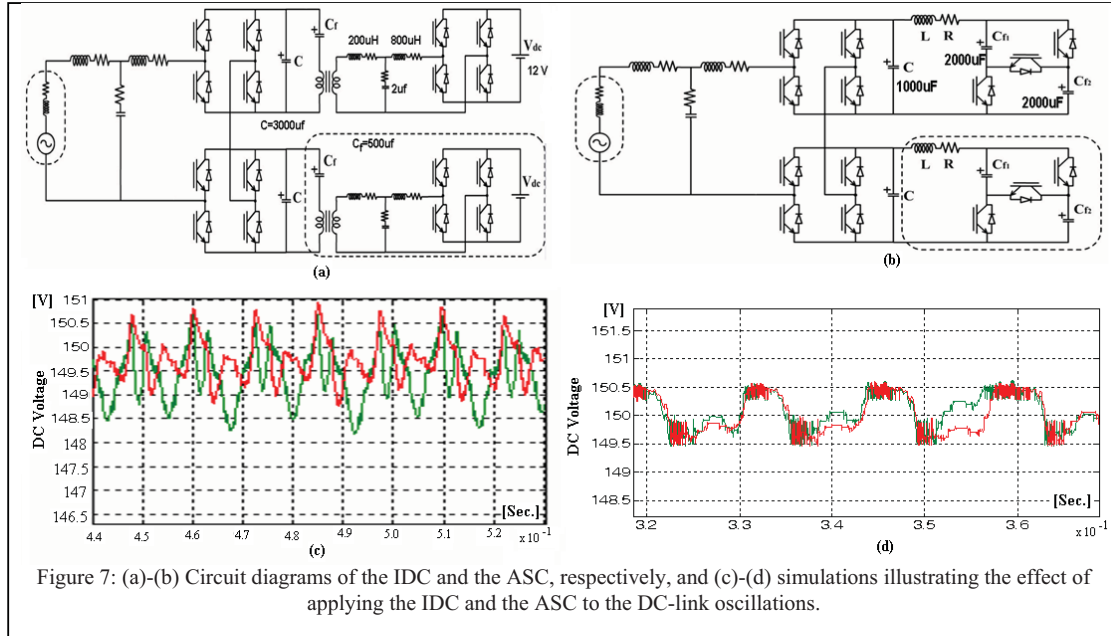


Figure 7: (a)-(b) Circuit diagrams of the IDC and the ASC, respectively, and (c)-(d) simulations illustrating the effect of applying the IDC and the ASC to the DC-link oscillations.

Where V_L is the voltage drop on inductance L and i_L is the absorbed current. This relatively big slope forces the main DC-link voltage to come down more rapidly. Similarly, when the DC-link voltage is dropped below a negative band ($-\Delta V$), the two vertical switches are turned off and the horizontal switch turns on. The two capacitors C_{f1} and C_{f2} operate in series, injecting current to the DC-link capacitor C through the inductance L as follows:

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{V_{DC} - \frac{6}{4}V_{DC}}{L} = -\frac{V_{DC}}{2L} \quad (5)$$

Here the negative slope reverses the current from C_{f1} and C_{f2} to charge the DC-link capacitor C . Simulations show that peak-to-peak magnitude of the oscillations is smaller than 1 V (or 0.6%) for a very high switching frequency case as shown in Fig. 6(d). In practice, the hysteresis-band could limit the performance of the S-bridge considerably such that when the selected ΔV is small, the switching frequency is very high.

4.3 An equivalent buck-boost circuit: proposition 3

The two foregoing propositions have the advantage of lowering oscillations, while being forced to operate in high switching frequencies. In practise, this will highly depend on how fast and how advanced the semiconductor technology is. Also,

capacitor and a DC battery. Figure 7(a) demonstrates this proposal that mimics the oscillations of the DC-link using a rectifier. A full-wave diode rectifier supplies a DC voltage (V_{DC}) containing an average voltage (V_{mean}) plus a dominant 100 Hz oscillation (ΔV) to a load. A buck-boost circuit is used to compensate these emulated low-frequency oscillations.

Buck and boost operation modes take place when using two switches (one controllable switch and a diode allocated in each branch). Duty ratios of the switches are decided on the basis of pulse width modulation provided by Fig. 7(b), where V_{dc} is the battery voltage. When V_{DC} is dropping, the DC battery injects power to the DC-link (boost-mode); when V_{DC} is increasing, the DC battery absorbs power from the DC-link (buck-mode). This rule is emulated in Fig. 7(b), wherein a 50 kHz ramp is compared with V_{dc}/V_{mean} for the buck-mode, and $1 - V_{dc}/V_{mean}$ for the boost-mode. These are actually obtained from the well-known theory of DC-DC converters [12]. Simulations are shown in Figs. 7(c)-(d) wherein the last picture zooms on a small region of Fig. 7(c). It can be seen that the effective value of uncompensated oscillations efficiency drops down drastically. Practically speaking, the buck-boost compensation method is simple to implement, and that the oscillations can be traced properly. In the mean time, the cost of this design is much less than

the other two suggestions that use the concept of passive LC-filter compensation.

frequency estimation techniques. Further, the source equivalent impedance is needed to be included in the

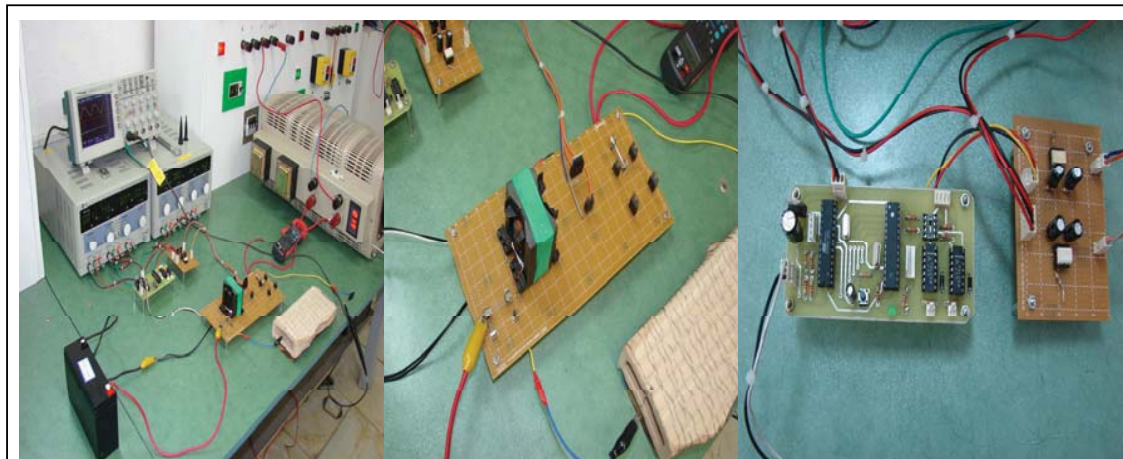
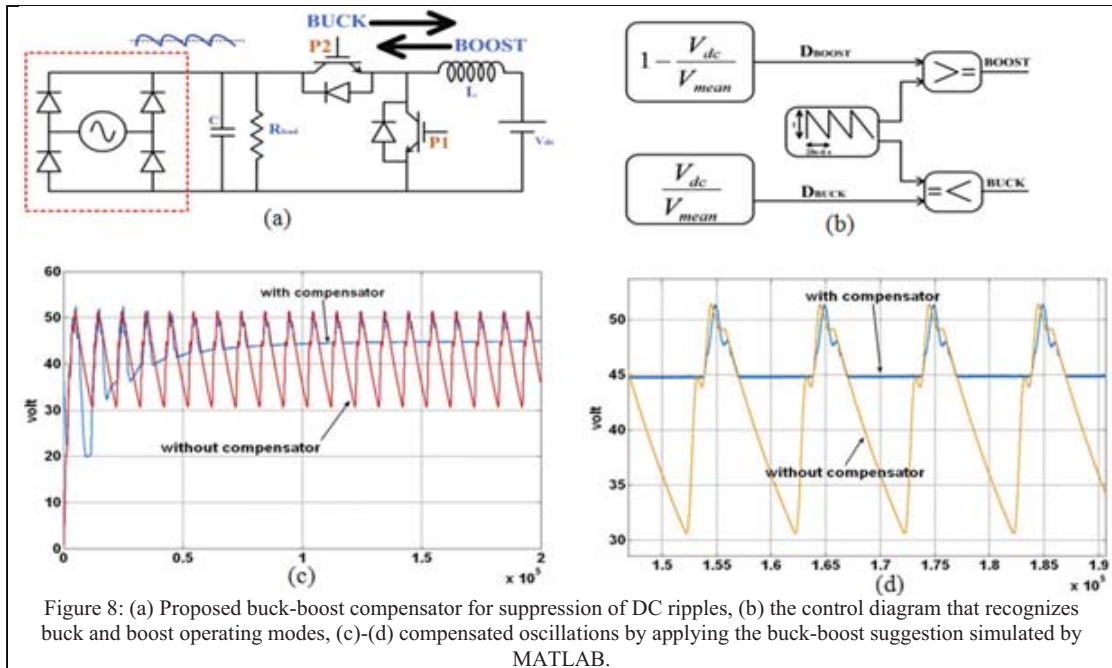


Figure 9: Experimental arrangement for suppression of low-frequency DC-link oscillations using the buck-boost proposition.

4.3.1 Implementation of the buck-boost proposal

The third proposition is implemented as the developed device is shown in Figs. 8(a)-(c). The power circuit along with control design of Fig. 7 is used to generate low-frequency oscillations by a full-bridge diode-rectifier. Supplied DC voltage by this full-wave rectifier basically provides an uneasy situation in which suppression of the produced oscillations need considerable attenuations compared to the DC-link oscillations of cascaded converter. It is noticeable that an exact cascaded converter can also be connected across the grid system, which will need additional control algorithms both for compensation approach and the synchronizing

control algorithm for a reliable response. This would be an extensive practical field, which needs the well-known FACTS controller techniques for shunt grid-connected devices. Hence, this made us to think about producing oscillations with the same frequency as that of the cascaded converter by establishing the test circuit of a full-bridge rectifier. The rectifier is composed of four 30 A diodes that are connected to a 133 μ F capacitor in parallel with an 18 Ω resistor. Two power MOSFETs (P50NE1) are used in the buck-boost circuit, which are driven by the IC driver TLP250.

Considering the compensating circuit in Fig. 7(a), the full-bridge rectifier generates a DC voltage that

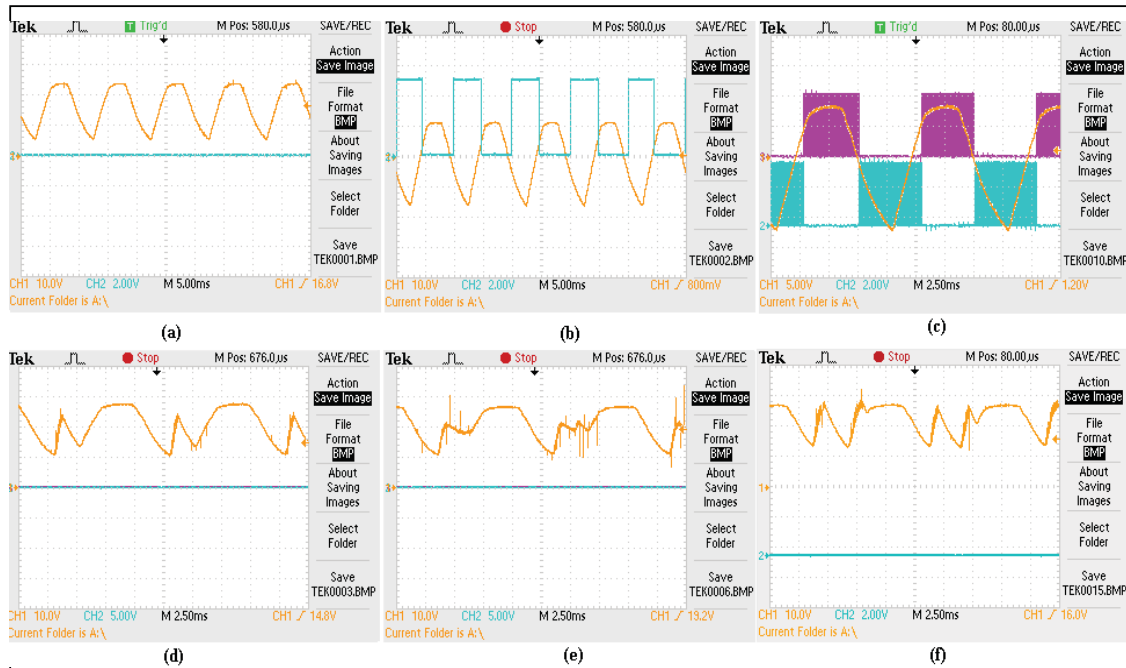


Figure 10: (a) Generated 100 Hz oscillations by the full-bridge rectifier, (b) recognition of buck/boost operation modes, (c) the switching patterns generated for both buck and boost modes, (d)-(f) suppression of oscillations using the FD, VC and WD, respectively.

contains significant 100 Hz ripples. The peak of these ripples is imposed by the rectifier such that compensation circuits have to suppress the oscillations with respect to the peak (not the average). Thus, this situation would be rather a difficult task compared to the exact cascaded converter application. The microcontroller is programmed in three controlled-cases for suppression of oscillations; fixed duty-cycle modulation (FD), voltage-controlled modulation (VC) and wider-band boost duty-cycle modulation (WD).

Experimental results are shown in Fig. 9. Figure 9(a) introduces the generated 100 Hz oscillations by the full-bridge rectifier. The DC value of this voltage is 15.00 V, while the RMS value of ripples is 20.90 V. Figure 9(b) illustrates the recognition of buck and boost operating modes according to the control rule shown in Fig. 7 (zero for the buck mode, and 5 V for the boost mode). The switching pulse train for each of the two operating modes are shown in Fig. 9(c). The upper switching signals relate to the activation of boost converter, and the lower ones to the activation of buck converter.

Considering the FD modulation for the buck-boost, Fig. 9(d) demonstrates the resultant compensation of DC oscillations (ΔV). It can be seen that the buck-boost effectively suppresses the ripples such that the RMS of the oscillations is 4.689 V.

Comparing this RMS value with that of the initial rectifier DC ripples (20.90 V), buck-boost compensator along with the FD modulation reduces the RMS value of the oscillations down by 77.52%. Meanwhile, the DC value of the rectifier output is raised up to 20.89 V. Application of the VC modulation to the buck-boost is recorded in Fig. 9(e) in which the duty ratio is regulated proportionally with respect to the mean value of the DC voltage. The RMS value of the oscillation is lowered down to 4.103 V, leading to the DC voltage rise up to 20.62 V. This shows slightly better performance than that of the FD modulation that reduces the effective value of the initial DC ripples down by 80.37%. Finally, the WD modulation is applied to the buck-boost compensator in which a wider-band is assigned to the boost converter. The RMS value of the oscillations and the DC value are 4.459 V and 21.94 V, respectively. Comparing with other two methods, the WD modulation introduces 78.67% reduction in the RMS magnitude of the oscillations, presenting the highest DC value.

5- Conclusion

Two problems are discussed in this paper in conjunction with cascaded H-bridge converters. The first issue deals with uneven distribution of the applied AC voltage on the H-bridge sub-modules due

to the engaged modulation technique. Second problem is related to a dominant 100/120 Hz oscillation on the DC-links because of active power exchange between AC and DC sides. Oscillations are then modulated by the converter, injecting undesirable uncharacteristic harmonics to the AC system. Furthermore, the DC voltages of the cascaded converters will *not* oscillate together, and this produces further sub-modules' DC voltage unbalance. To overcome the first problem, a switching pulse transposition procedure is suggested for conventional SPWM along with the optimal PWM modulation techniques. Suggestions are then verified using a practical five-level converter that is implemented by cascading two H-bridge converters, showing a significant improvement in AC voltage distribution. Further, to suppress the DC-link oscillations, three compensating circuits are proposed, which are the independent DC source, the auxiliary S-bridge and the buck-boost converter design. While all suggested circuits effectively reduce the oscillations, the low-cost buck-boost converter is the most inexpensive design. Hence, a buck-boost design is arranged and tested under certain oscillations. Duty ratios of the switches are regulated using three different methods. Experimental results confirm that the effective values of the DC-link oscillations are lowered significantly compared to the uncompensated case.

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