

LM3940 1A Low Dropout Regulator for 5V to 3.3V Conversion

 Check for Samples: [LM3940](#)

FEATURES

- Output voltage specified over temperature
- Excellent load regulation
- Specified 1A output current
- Requires only one external component
- Built-in protection against excess temperature
- Short circuit protected

APPLICATIONS

- Laptop/Desktop Computers
- Logic Systems

DESCRIPTION

The LM3940 is a 1A low dropout regulator designed to provide 3.3V from a 5V supply.

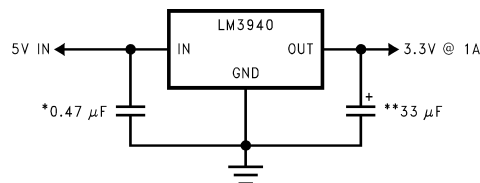
The LM3940 is ideally suited for systems which contain both 5V and 3.3V logic, with prime power provided from a 5V bus.

Because the LM3940 is a true low dropout regulator, it can hold its 3.3V output in regulation with input voltages as low as 4.5V.

The TO-220 package of the LM3940 means that in most applications the full 1A of load current can be delivered without using an additional heatsink.

The surface mount DDPAK/TO-263 package uses minimum board space, and gives excellent power dissipation capability when soldered to a copper plane on the PC board.

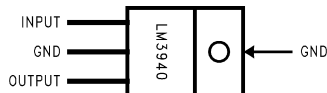
TYPICAL APPLICATION



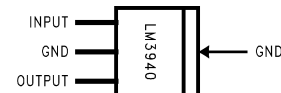
*Required if regulator is located more than 1" from the power supply filter capacitor or if battery power is used.

**See [APPLICATION HINTS](#).

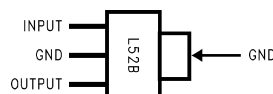
CONNECTION DIAGRAM



**Figure 1. 3-Lead TO-220 Package
(Front View)**
Drawing Number NDE00EB



**Figure 2. 3-Lead DDPAK/TO-263 Package
(Front View)**
Drawing Number KTT003B

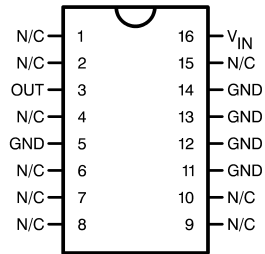


**Figure 3. 3-Lead SOT-223
(Front View)**
Drawing Number DCY (R-PDSO-G4)

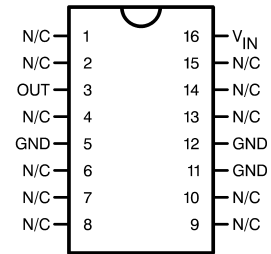


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

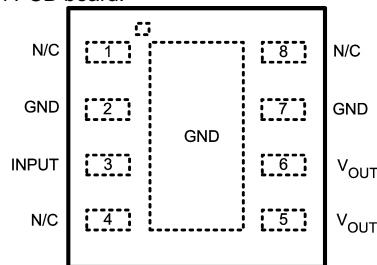


**Figure 4. 16-Lead CDIP
(Top View)
Drawing Number NFE0016A**



**Figure 5. 16-Lead CLGA
(Top View)
Drawing Number NAC0016A**

- A. Pin 2 and pin 7 are fused to center DAP.
- B. Pin 5 and 6 need to be tied together on PCB board.



**Figure 6. 8-Lead WSON
(Top View)^{(A)(B)}
Drawing Number NGN008A**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|---|--------------------|
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (Soldering, 5 seconds) | 260°C |
| Power Dissipation ⁽²⁾ | Internally Limited |
| Input Supply Voltage | 7.5V |
| ESD Rating ⁽³⁾ | 2 kV |

- (1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
- (2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J , the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. The value of θ_{JA} (for devices in still air with no heatsink) is 60°C/W for the TO-220 package, 80°C/W for the DPAK/TO-263 package, and 174°C/W for the SOT-223 package. The effective value of θ_{JA} can be reduced by using a heatsink (see [APPLICATION HINTS](#) for specific information on heatsinking). The value of θ_{JA} for the WSON package is specifically dependant on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 [SNOA401](#). The θ_{JA} rating for the WSON is with a JESD51-7 test board having 6 thermal vias under the exposed pad.
- (3) ESD rating is based on the human body model: 100 pF discharged through 1.5 kΩ.

Operating Ratings⁽¹⁾

| | |
|-------------------------------------|-----------------|
| Junction Temperature Range, T_J | -40°C to +125°C |
| Input Supply Voltage, $V_{IN(MIN)}$ | $V_O + V_{DO}$ |

- (1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for $T_J = 25^\circ\text{C}$, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = 5\text{V}$, $I_L = 1\text{A}$, $C_{OUT} = 33\ \mu\text{F}$.

| Symbol | Parameter | Conditions | Typical | LM3940 ⁽¹⁾ | | Units |
|-------------------------------------|--------------------------------|---|---------|-----------------------|---------------------|---------------------|
| | | | | min | max | |
| V_O | Output Voltage | $5\ \text{mA} \leq I_L \leq 1\ \text{A}$ | 3.3 | 3.20 3.13 | 3.40 3.47 | V |
| $\frac{\Delta V_O}{\Delta V_I}$ (1) | Line Regulation | $I_L = 5\ \text{mA}$ $4.5\text{V} \leq V_{IN} \leq 5.5\text{V}$ | 20 | | 40 | mV |
| $\frac{\Delta V_O}{I_L}$ (2) | Load Regulation | $50\ \text{mA} \leq I_L \leq 1\ \text{A}$ | 35 | | 50 80 | |
| Z_O | Output Impedance | I_L (DC) = 100 mA I_L (AC) = 20 mA (rms) $f = 120\ \text{Hz}$ | 35 | | | m Ω |
| I_Q | Quiescent Current | $4.5\text{V} \leq V_{IN} \leq 5.5\text{V}$ $I_L = 5\ \text{mA}$ | 10 | | 15 20 | mA |
| | | $V_{IN} = 5\text{V}$ $I_L = 1\ \text{A}$ | 110 | | 200 250 | |
| e_n | Output Noise Voltage | BW = 10 Hz–100 kHz $I_L = 5\ \text{mA}$ | 150 | | | μV (rms) |
| V_{DO} | Dropout Voltage ⁽²⁾ | $I_L = 1\ \text{A}$ | 0.5 | | 0.8 1.0 | V |
| | | $I_L = 100\ \text{mA}$ | 110 | | 150 200 | mV |
| $I_L(\text{SC})$ | Short Circuit Current | $R_L = 0$ | 1.7 | 1.2 | | A |

- (1) All limits specified for $T_J = 25^\circ\text{C}$ are 100% tested and are used to calculate Outgoing Quality Levels. All limits at temperature extremes are verified via correlation using standard Statistical Quality Control (SQC) methods.
- (2) Dropout voltage is defined as the input-output differential voltage where the regulator output drops to a value that is 100 mV below the value that is measured at $V_{IN} = 5\text{V}$.

THERMAL PERFORMANCE

| | | | |
|--|----------------------------|----|---------------------------|
| Thermal Resistance, Junction-to-Case, θ_{JC} | 3-Lead TO-220 | 4 | $^\circ\text{C}/\text{W}$ |
| | 3-Lead DDPAK/TO-263 | 4 | $^\circ\text{C}/\text{W}$ |
| | 8-Lead WSON | 6 | $^\circ\text{C}/\text{W}$ |
| Thermal Resistance, Junction-to-Ambient, θ_{JA} | 3-Lead TO-220 | 60 | $^\circ\text{C}/\text{W}$ |
| | 3-Lead DDPAK/TO-263 | 80 | $^\circ\text{C}/\text{W}$ |
| | 8-Lead WSON ⁽¹⁾ | 35 | $^\circ\text{C}/\text{W}$ |

- (1) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J , the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. The value of θ_{JA} (for devices in still air with no heatsink) is $60^\circ\text{C}/\text{W}$ for the TO-220 package, $80^\circ\text{C}/\text{W}$ for the DDPAK/TO-263 package, and $174^\circ\text{C}/\text{W}$ for the SOT-223 package. The effective value of θ_{JA} can be reduced by using a heatsink (see [APPLICATION HINTS](#) for specific information on heatsinking). The value of θ_{JA} for the WSON package is specifically dependant on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 [SNOA401](#). The θ_{JA} rating for the WSON is with a JESD51-7 test board having 6 thermal vias under the exposed pad.

TYPICAL PERFORMANCE CHARACTERISTICS

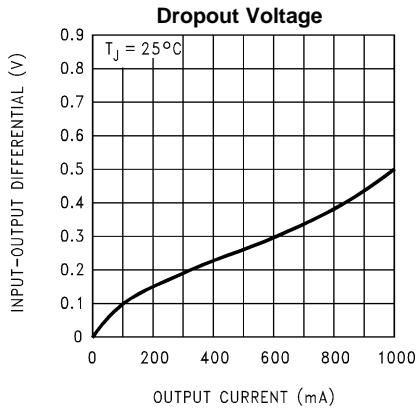


Figure 7.

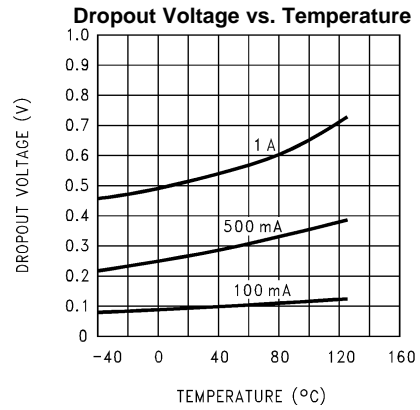


Figure 8.

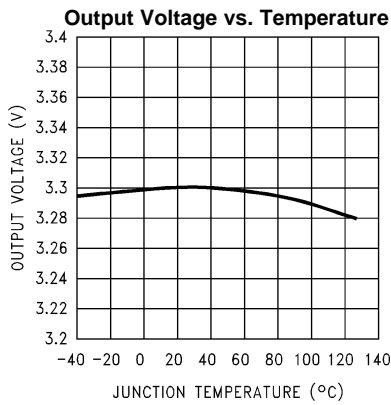


Figure 9.

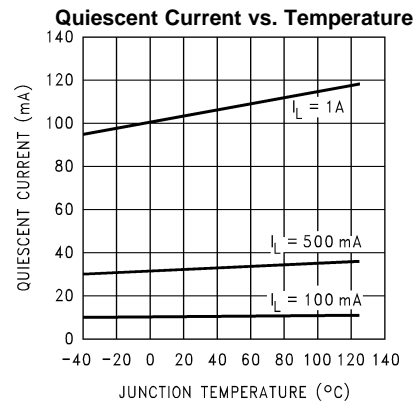


Figure 10.

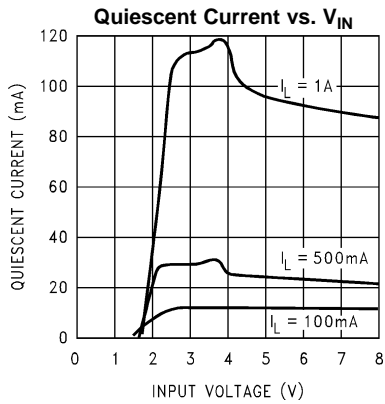


Figure 11.

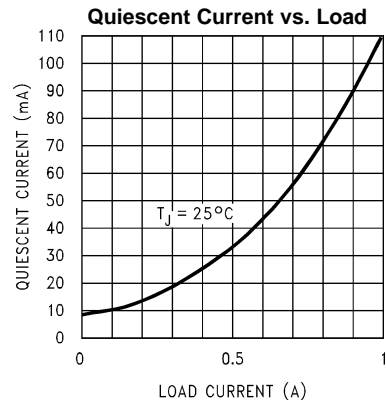


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

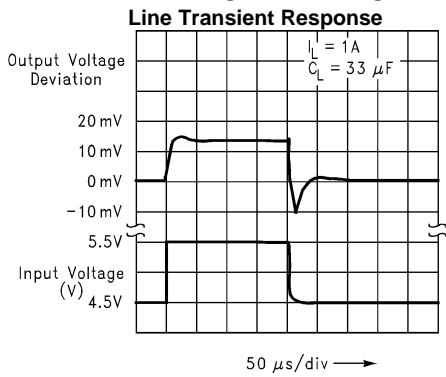


Figure 13.

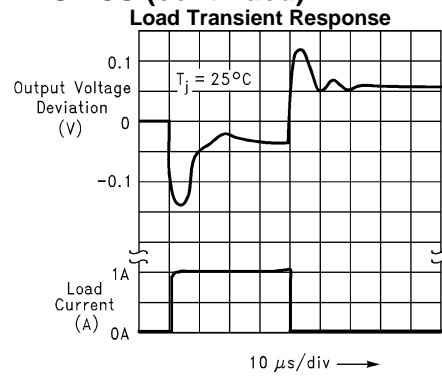


Figure 14.

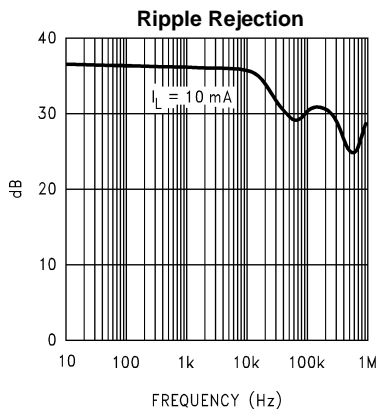


Figure 15.

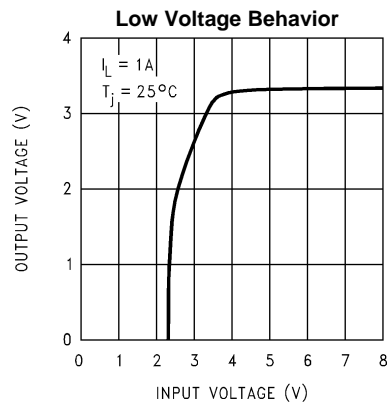


Figure 16.

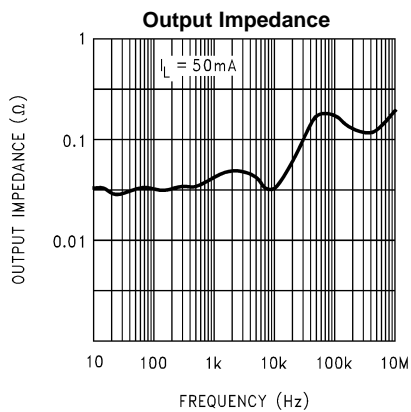


Figure 17.

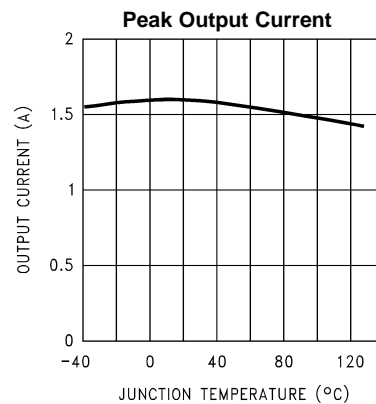


Figure 18.

APPLICATION HINTS

EXTERNAL CAPACITORS

The output capacitor is critical to maintaining regulator stability, and must meet the required conditions for both ESR (Equivalent Series Resistance) and minimum amount of capacitance.

MINIMUM CAPACITANCE:

The minimum output capacitance required to maintain stability is 33 μF (this value may be increased without limit). Larger values of output capacitance will give improved transient response.

ESR LIMITS:

The ESR of the output capacitor will cause loop instability if it is too high or too low. The acceptable range of ESR plotted versus load current is shown in [Figure 19](#). ***It is essential that the output capacitor meet these requirements, or oscillations can result.***

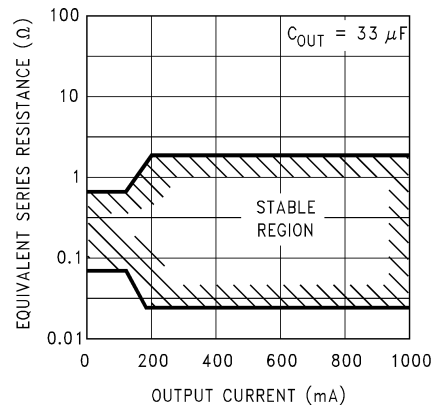


Figure 19. ESR Limits

It is important to note that for most capacitors, ESR is specified only at room temperature. However, the designer must ensure that the ESR will stay inside the limits shown over the entire operating temperature range for the design.

For aluminum electrolytic capacitors, ESR will increase by about 30X as the temperature is reduced from 25°C to -40°C. This type of capacitor is not well-suited for low temperature operation.

Solid tantalum capacitors have a more stable ESR over temperature, but are more expensive than aluminum electrolytics. A cost-effective approach sometimes used is to parallel an aluminum electrolytic with a solid Tantalum, with the total capacitance split about 75/25% with the Aluminum being the larger value.

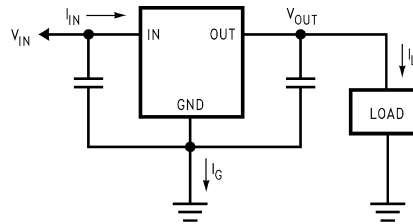
If two capacitors are paralleled, the effective ESR is the parallel of the two individual values. The “flatter” ESR of the Tantalum will keep the effective ESR from rising as quickly at low temperatures.

HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under [Absolute Maximum Ratings](#).

To determine if a heatsink is required, the power dissipated by the regulator, P_D , must be calculated.

[Figure 20](#) shows the voltages and currents which are present in the circuit, as well as the formula for calculating the power dissipated in the regulator:



$$I_{IN} = I_L + I_G$$

$$P_D = (V_{IN} - V_{OUT}) I_L + (V_{IN}) I_G$$

Figure 20. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, T_R (max). This is calculated by using the formula:

$$T_R \text{ (max)} = T_J \text{ (max)} - T_A \text{ (max)}$$

Where: T_J (max) is the maximum allowable junction temperature, which is 125°C for commercial grade parts.

T_A (max) is the maximum ambient temperature which will be encountered in the application.

Using the calculated values for T_R (max) and P_D , the maximum allowable value for the junction-to-ambient thermal resistance, $\theta_{(JA)}$, can now be found:

$$\theta_{(JA)} = T_R \text{ (max)}/P_D$$

IMPORTANT: If the maximum allowable value for $\theta_{(JA)}$ is found to be $\geq 60^\circ\text{C}/\text{W}$ for the TO-220 package, $\geq 80^\circ\text{C}/\text{W}$ for the DDPAK/TO-263 package, or $\geq 174^\circ\text{C}/\text{W}$ for the SOT-223 package, no heatsink is needed since the package alone will dissipate enough heat to satisfy these requirements.

If the calculated value for $\theta_{(JA)}$ falls below these limits, a heatsink is required.

HEATSINKING TO-220 PACKAGE PARTS

The TO-220 can be attached to a typical heatsink, or secured to a copper plane on a PC board. If a copper plane is to be used, the values of $\theta_{(JA)}$ will be the same as shown in the [HEATSINKING TO-263](#) section for the DDPAK/TO-263.

If a manufactured heatsink is to be selected, the value of heatsink-to-ambient thermal resistance, $\theta_{(H-A)}$, must first be calculated:

$$\theta_{(H-A)} = \theta_{(JA)} - \theta_{(C-H)} - \theta_{(J-C)}$$

Where: $\theta_{(J-C)}$ is defined as the thermal resistance from the junction to the surface of the case. A value of 4°C/W can be assumed for $\theta_{(J-C)}$ for this calculation.

$\theta_{(C-H)}$ is defined as the thermal resistance between the case and the surface of the heatsink. The value of $\theta_{(C-H)}$ will vary from about 1.5°C/W to about 2.5°C/W (depending on method of attachment, insulator, etc.). If the exact value is unknown, 2°C/W should be assumed for $\theta_{(C-H)}$.

When a value for $\theta_{(H-A)}$ is found using the equation shown above, *a heatsink must be selected that has a value that is less than or equal to this number.*

$\theta_{(H-A)}$ is specified numerically by the heatsink manufacturer in the catalog, or shown in a curve that plots temperature rise vs. power dissipation for the heatsink.

HEATSINKING DDPAK/TO-263 AND SOT-223 PACKAGE PARTS

Both the DDPAK/TO-263 (“KTT”) and SOT-223 (“DCY”) packages use a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

[Figure 21](#) shows for the DDPAK/TO-263 the measured values of $\theta_{(JA)}$ for different copper sizes using a typical PCB with 1 ounce copper *and no solder mask over the copper area used for heatsinking.*

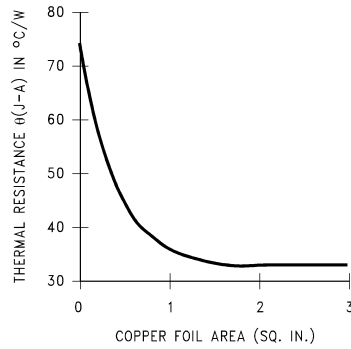


Figure 21. $\theta_{(JA)}$ vs. Copper (1 ounce) Area for the DDPAK/TO-263 Package

As shown in [Figure 21](#), increasing the copper area beyond 1 square inch produces very little improvement. It should also be observed that the minimum value of $\theta_{(JA)}$ for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

As a design aid, [Figure 22](#) shows the maximum allowable power dissipation compared to ambient temperature for the DDPAK/TO-263 device (assuming $\theta_{(JA)}$ is 35°C/W and the maximum junction temperature is 125°C).

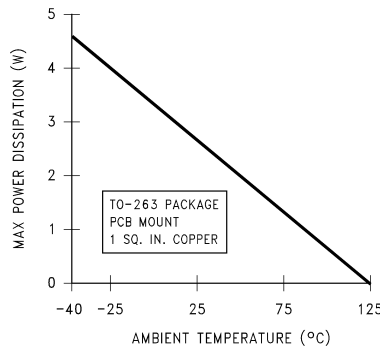


Figure 22. Maximum Power Dissipation vs. T_{AMB} for the DDPAK/TO-263 Package

[Figure 23](#) and [Figure 24](#) show the information for the SOT-223 package. [Figure 24](#) assumes a $\theta_{(JA)}$ of 74°C/W for 1 ounce copper and 51°C/W for 2 ounce copper and a maximum junction temperature of 125°C.

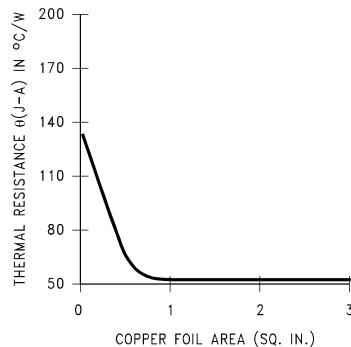


Figure 23. $\theta_{(JA)}$ vs. Copper (2 ounce) Area for the SOT-223 Package

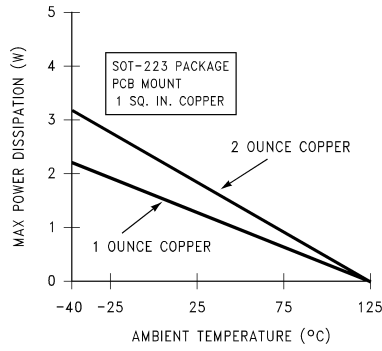


Figure 24. Maximum Power Dissipation vs. T_{AMB} for the SOT-223 Package

Please see AN1028 for power enhancement techniques to be used with the SOT-223 package.

REVISION HISTORY

| Changes from Revision D (March 2013) to Revision E | Page |
|--|-------------------|
| • Changed layout of National Data Sheet to TI format | 9 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---------------------|---------------|------------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| LM3940IMP-3.3 | ACTIVE | SOT-223 | DCY | 4 | 1000 | TBD | Call TI | Call TI | -40 to 125 | L52B | Samples |
| LM3940IMP-3.3/NOPB | ACTIVE | SOT-223 | DCY | 4 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L52B | Samples |
| LM3940IMPX-3.3 | ACTIVE | SOT-223 | DCY | 4 | 2000 | TBD | Call TI | Call TI | -40 to 125 | L52B | Samples |
| LM3940IMPX-3.3/NOPB | ACTIVE | SOT-223 | DCY | 4 | 2000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L52B | Samples |
| LM3940IS-3.3 | ACTIVE | DDPAK/ TO-263 | KTT | 3 | 45 | TBD | Call TI | Call TI | -40 to 125 | LM3940IS -3.3 P+ | Samples |
| LM3940IS-3.3/NOPB | ACTIVE | DDPAK/ TO-263 | KTT | 3 | 45 | Pb-Free (RoHS Exempt) | CU SN | Level-3-245C-168 HR | -40 to 125 | LM3940IS -3.3 P+ | Samples |
| LM3940ISX-3.3 | ACTIVE | DDPAK/ TO-263 | KTT | 3 | 500 | TBD | Call TI | Call TI | -40 to 125 | LM3940IS -3.3 P+ | Samples |
| LM3940ISX-3.3/NOPB | ACTIVE | DDPAK/ TO-263 | KTT | 3 | 500 | Pb-Free (RoHS Exempt) | CU SN | Level-3-245C-168 HR | -40 to 125 | LM3940IS -3.3 P+ | Samples |
| LM3940IT-3.3 | ACTIVE | TO-220 | NDE | 3 | 45 | TBD | Call TI | Call TI | -40 to 125 | LM3940IT -3.3 P+ | Samples |
| LM3940IT-3.3/NOPB | ACTIVE | TO-220 | NDE | 3 | 45 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | -40 to 125 | LM3940IT -3.3 P+ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------------|------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM3940IMP-3.3 | SOT-223 | DCY | 4 | 1000 | 330.0 | 16.4 | 7.0 | 7.5 | 2.2 | 12.0 | 16.0 | Q3 |
| LM3940IMP-3.3/NOPB | SOT-223 | DCY | 4 | 1000 | 330.0 | 16.4 | 7.0 | 7.5 | 2.2 | 12.0 | 16.0 | Q3 |
| LM3940IMPX-3.3 | SOT-223 | DCY | 4 | 2000 | 330.0 | 16.4 | 7.0 | 7.5 | 2.2 | 12.0 | 16.0 | Q3 |
| LM3940IMPX-3.3/NOPB | SOT-223 | DCY | 4 | 2000 | 330.0 | 16.4 | 7.0 | 7.5 | 2.2 | 12.0 | 16.0 | Q3 |
| LM3940ISX-3.3 | DDPAK/ TO-263 | KTT | 3 | 500 | 330.0 | 24.4 | 10.75 | 14.85 | 5.0 | 16.0 | 24.0 | Q2 |
| LM3940ISX-3.3/NOPB | DDPAK/ TO-263 | KTT | 3 | 500 | 330.0 | 24.4 | 10.75 | 14.85 | 5.0 | 16.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM3940IMP-3.3 | SOT-223 | DCY | 4 | 1000 | 367.0 | 367.0 | 35.0 |
| LM3940IMP-3.3/NOPB | SOT-223 | DCY | 4 | 1000 | 367.0 | 367.0 | 35.0 |
| LM3940IMPX-3.3 | SOT-223 | DCY | 4 | 2000 | 367.0 | 367.0 | 35.0 |
| LM3940IMPX-3.3/NOPB | SOT-223 | DCY | 4 | 2000 | 367.0 | 367.0 | 35.0 |
| LM3940ISX-3.3 | DDPAK/TO-263 | KTT | 3 | 500 | 367.0 | 367.0 | 45.0 |
| LM3940ISX-3.3/NOPB | DDPAK/TO-263 | KTT | 3 | 500 | 367.0 | 367.0 | 45.0 |

NDE0003B



DCY (R-PDSO-G4)

PLASTIC SMALL-OUTLINE



- NOTES: A. All linear dimensions are in millimeters (inches).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC TO-261 Variation AA.

KTT0003B



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

| | |
|------------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Applications Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| | |
|-------------------------------|--|
| Automotive and Transportation | www.ti.com/automotive |
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Video and Imaging | www.ti.com/video |

TI E2E Community

e2e.ti.com

This datasheet has been downloaded from:

www.DatasheetCatalog.com

Datasheets for electronic components.