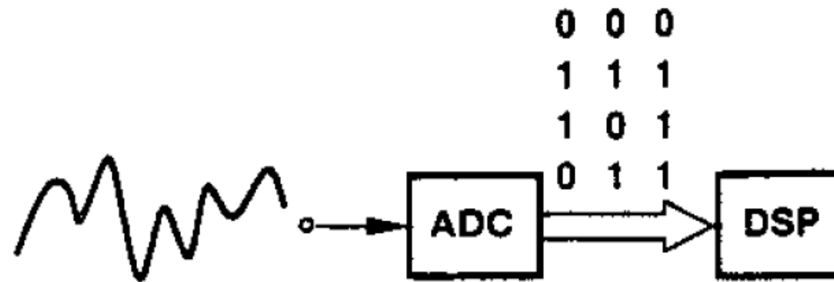
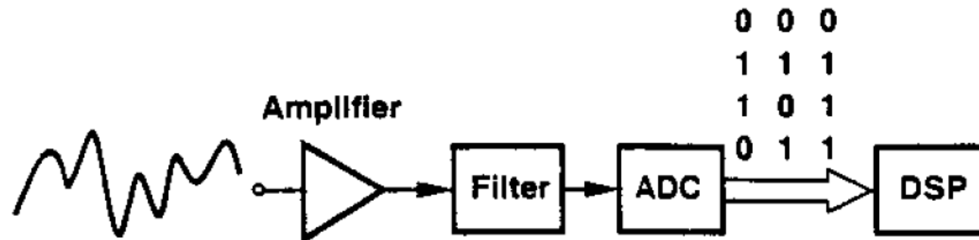
Analog Integrated Circuits

Hossein Shamsi

Why Analog?

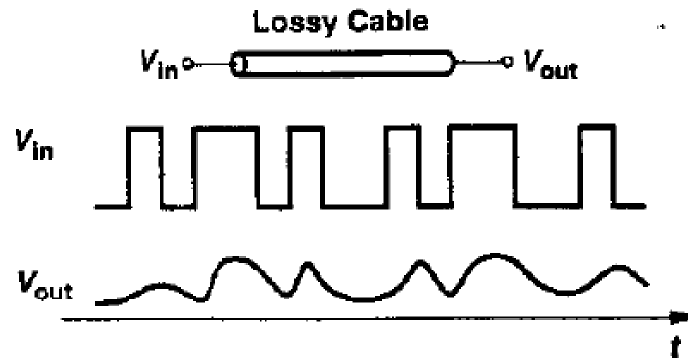
- Processing of Natural Signals





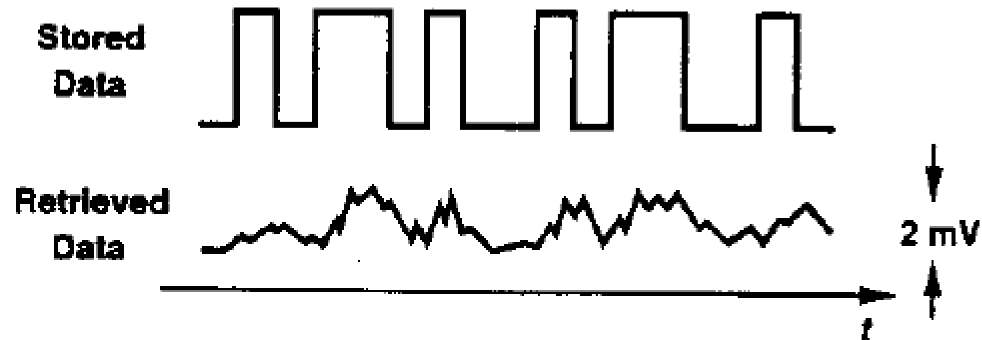
Why Analog?

- Digital Communication



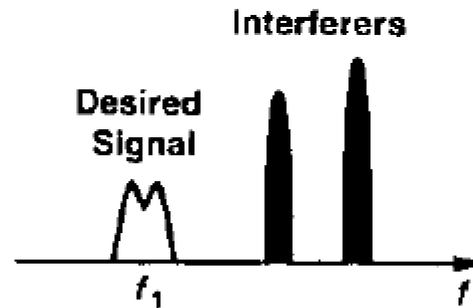
Why Analog?

- Disk Drive Electronics



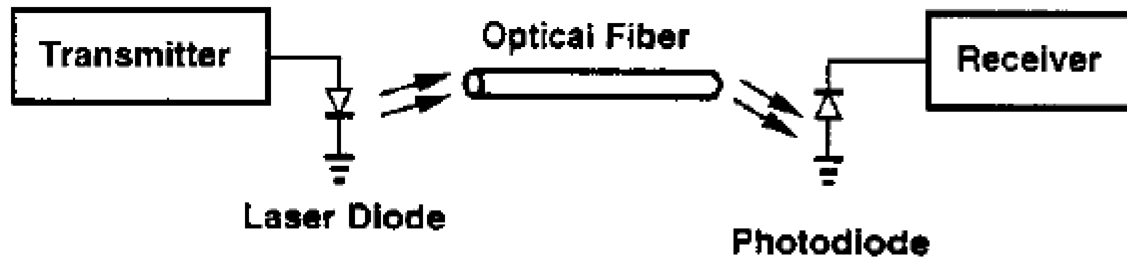
Why Analog?

- Wireless Receivers



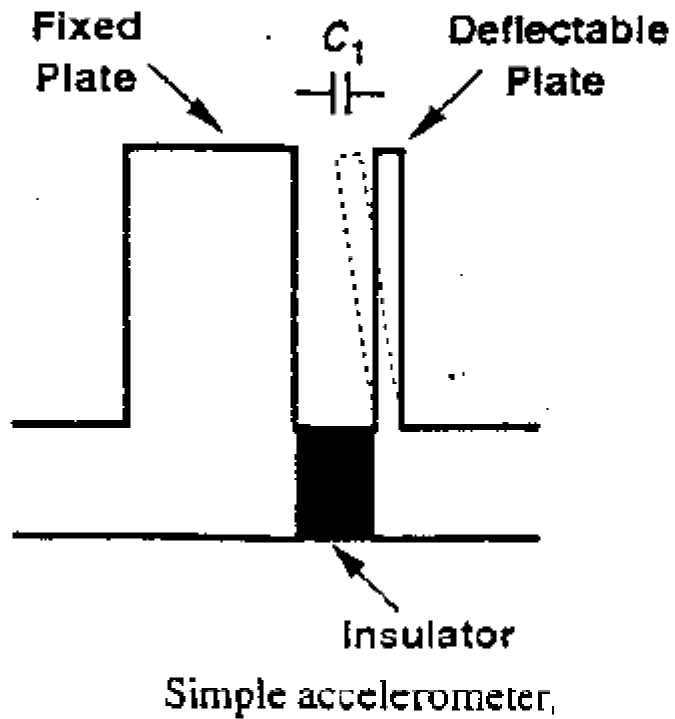
Why Analog?

- Optical Receivers

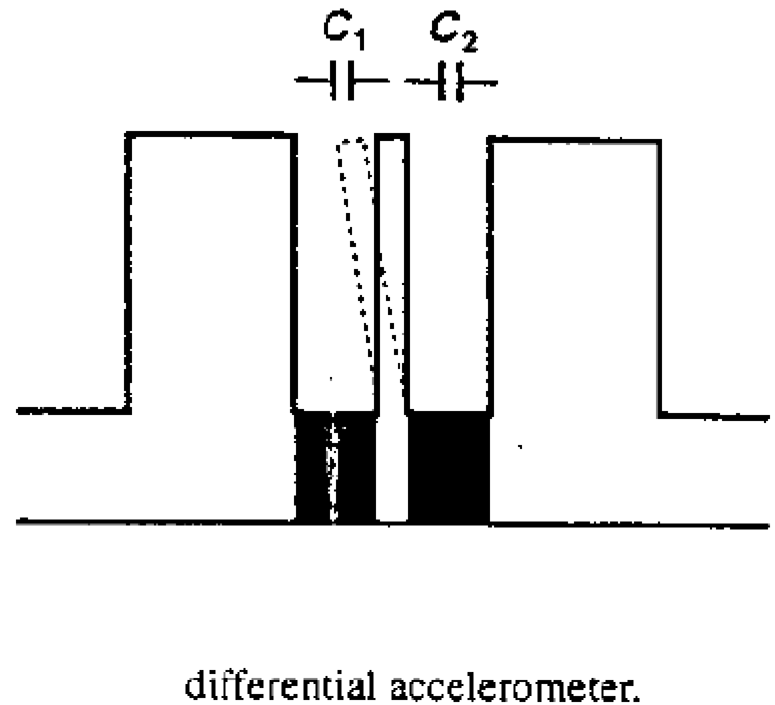


Why Analog?

- Sensors



Simple accelerometer,



differential accelerometer.

Why Analog?

- Microprocessors
  - Distribution and timing of data and clocks
  - Non-idealities in signal and power interconnects
  - Issues related to the package parasitics.
- Memories
  - They needs high-speed "sense amplifiers"

"High-speed digital design is in fact analog design."

Why Integrated?

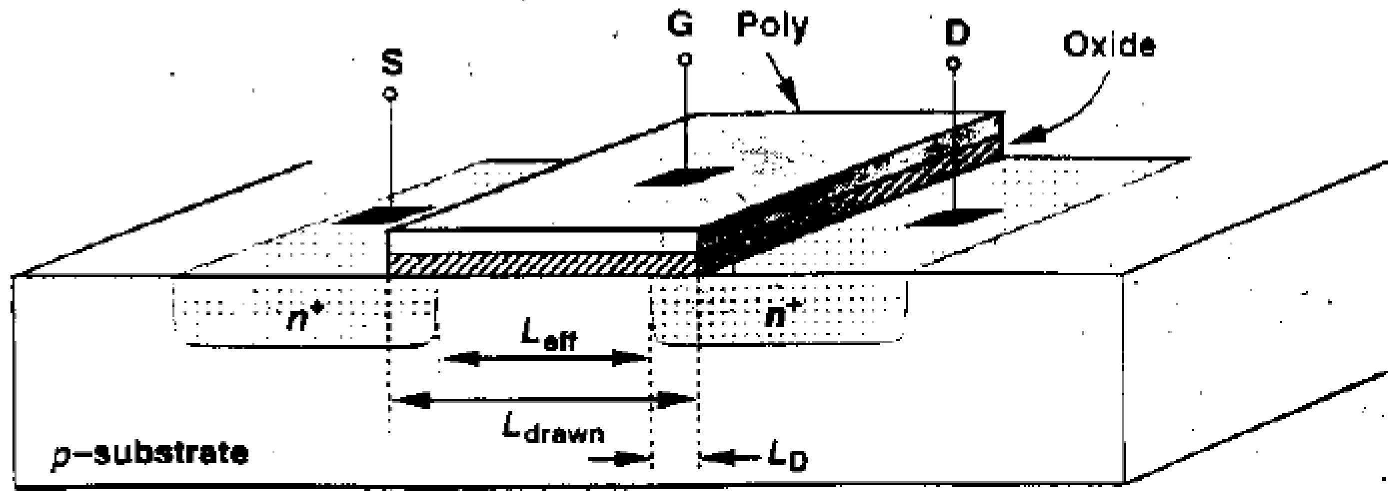
- The birthday of Electronics is 1900.
  - The main building block ➔ vacuum tube
  - Drawbacks
    - Large size
    - Small life-time
- The birthday of Microelectronics is 1960 (25µm Technology).
  - Microelectronics: the knowledge of integration of transistors in a small area.
  - The main building block ➔ Transistor
  - Advantages
    - small size
    - Infinite life-time
  - Moore's law: the number of transistors per chip has continued to double approximately every 1.5 years.
    - 25µm CMOS Technology ➔ 45nm CMOS Technology
  - CPU (3cm×3cm) ➔ 100-million transistors
  - Handset ➔ 1-million transistors
  - Memory ➔ 1-billion transistors
- The state-of-the-art microelectronics products:
  - Laptop
  - Cell phone
  - Digital camera

Why CMOS?

- Advantages:
  - CMOS technology is a low-power technology.
  - In order to realize digital circuits in CMOS technology, we need fewer devices than its Bipolar or GaAs counterparts.
- Disadvantages
  - Slower
  - Noisier

- Therefore CMOS technology is a helpful technology for digital circuits.
- Since we want to integrate both the analog and digital circuits on a same substrate, so we must design the analog circuits in CMOS technology.

Basic MOS Device Physics



Structure of a NMOS transistor

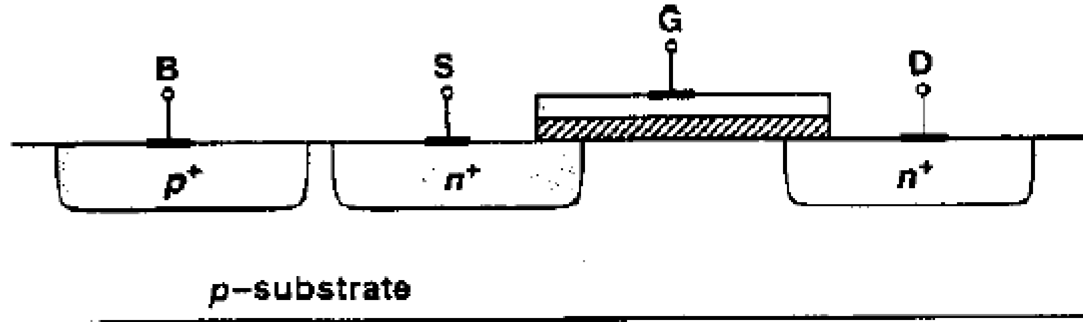
$$L_{eff} = L_{drawn} - 2L_D$$

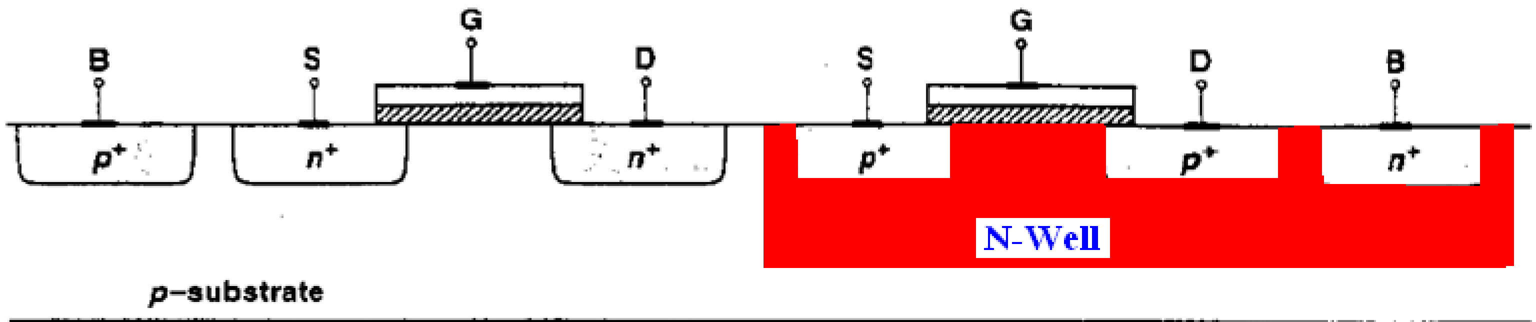
Typical values:

$L_{eff} = 10nm$

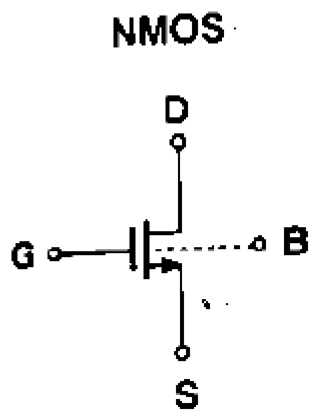
$t_{ox} = 1.5nm = 15A$

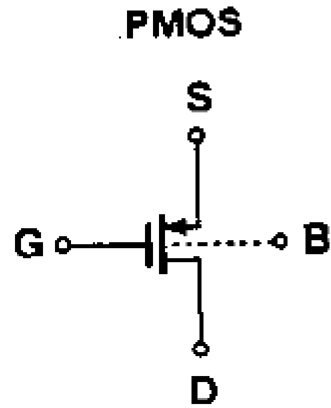
N-Well Process

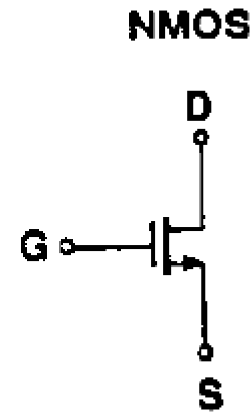


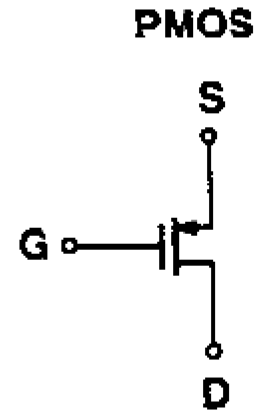


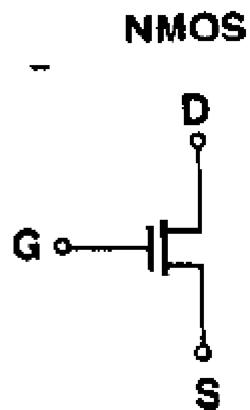
MOS Symbols

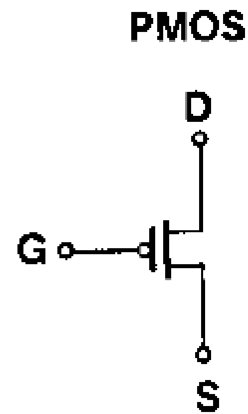




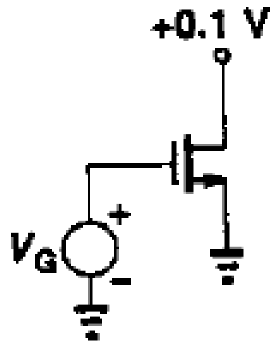


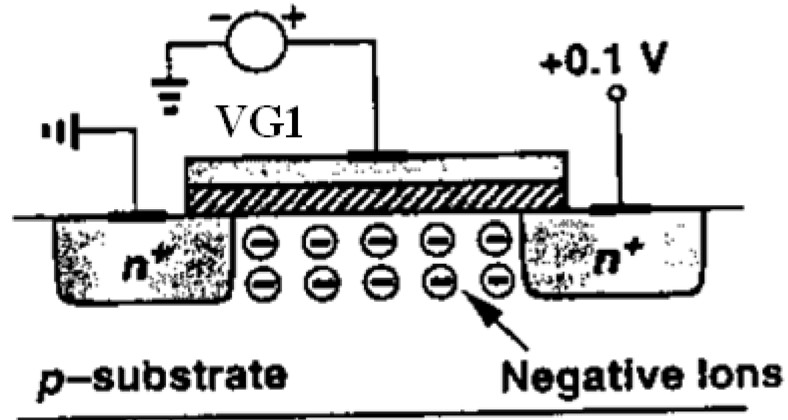






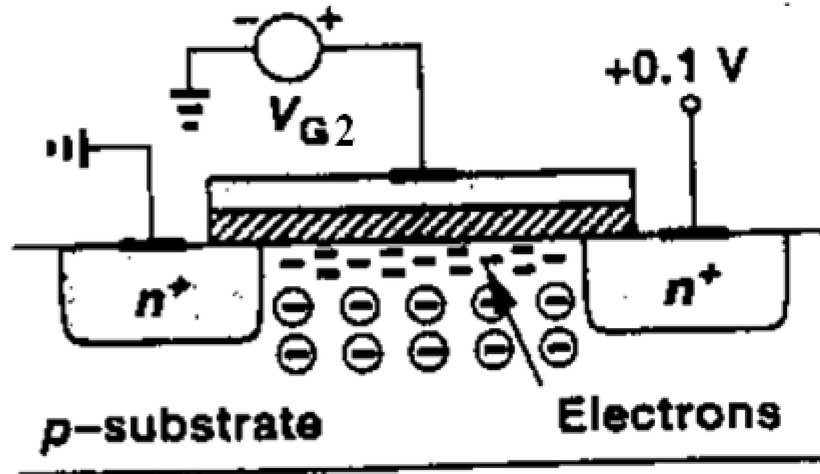
MOS I/V Characteristics





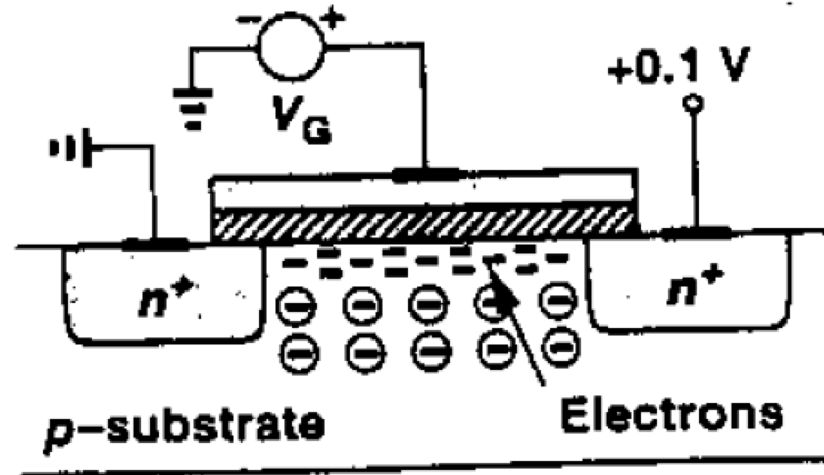
Formation of the depletion region

$$V_{G2} > V_{G1}$$



Formation of the inversion layer

MOS I/V Characteristics



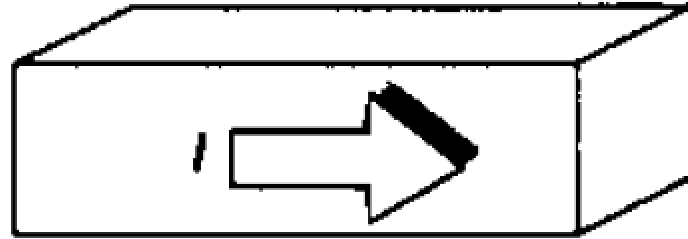
$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}},$$

$$\Phi_F = (kT/q)\ln(N_{sub}/n_i)$$

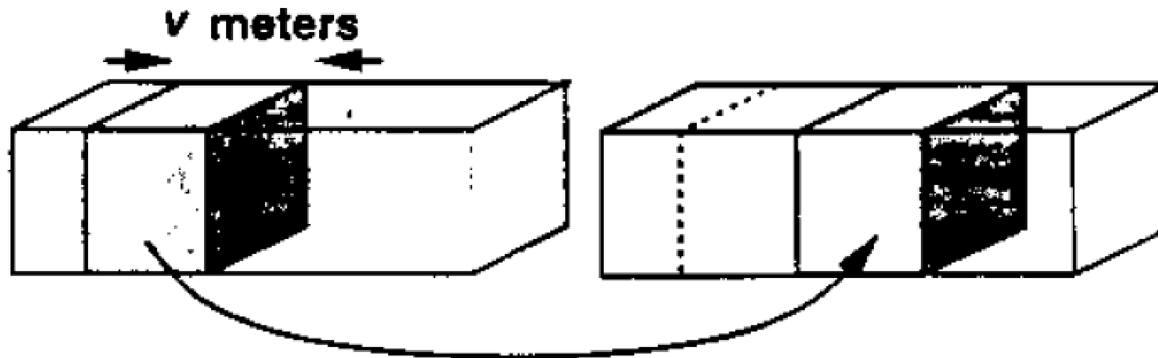
$$Q_{dep} = \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$$

$$for\ t_{ox} = 2nm, we\ have: C_{ox} = 17.25fF/\mu m^2$$

Derivation of I/V Characteristics



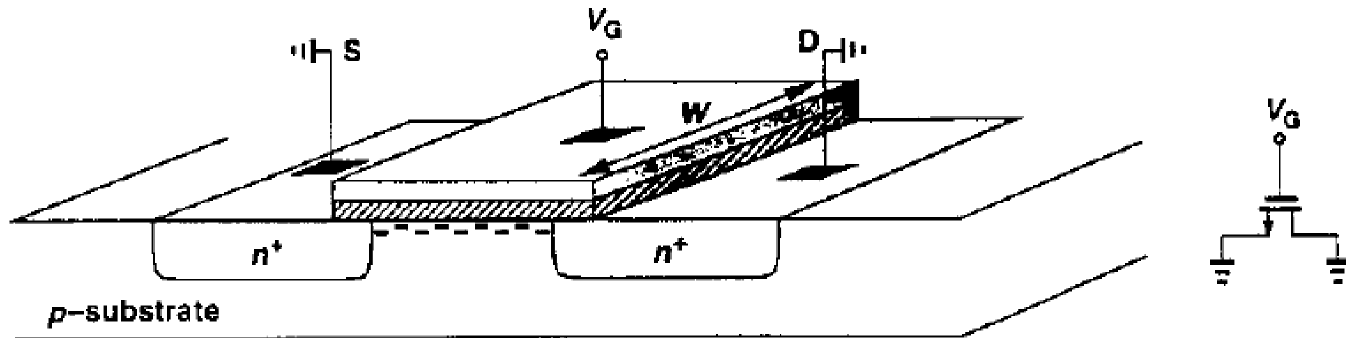
A semiconductor bar carrying a current **I**



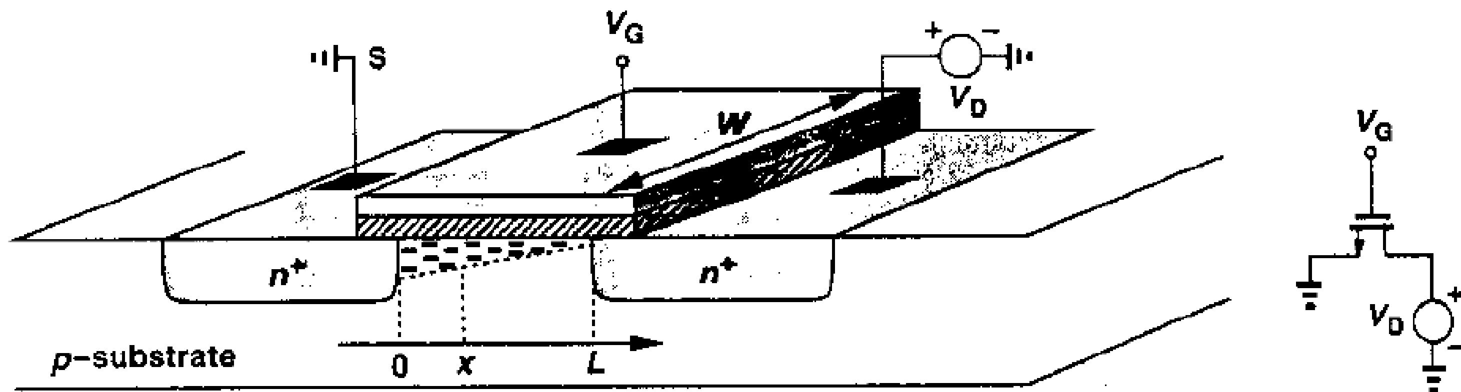
Snapshots of the carriers one second apart.

$$I = Q_d \cdot v.$$

Derivation of I/V Characteristics



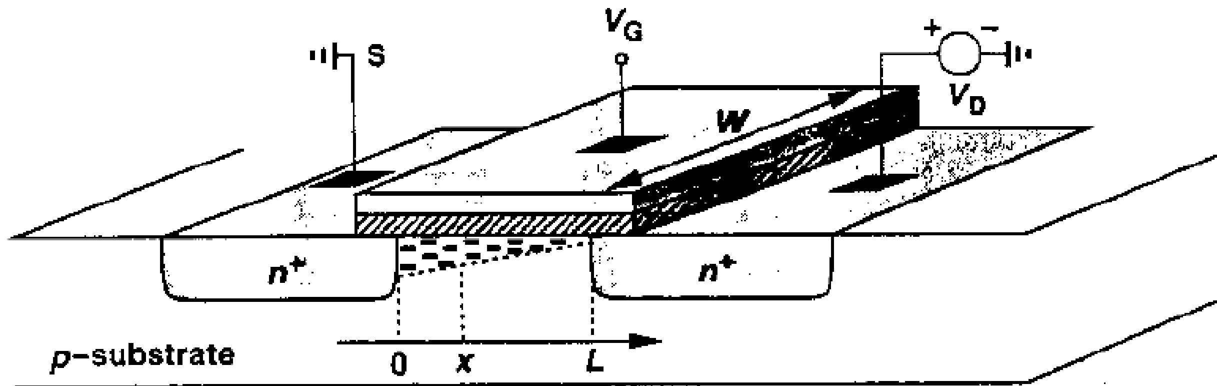
$$Q_d = -WC_{ox}\left(V_{GS} - V_{TH}\right)$$

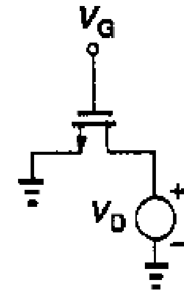


$$Q_d = -WC_{ox}\left[V_{G-Ch}(x) - V_{TH}\right] \Rightarrow Q_d = -WC_{ox}\left[V_G - V_{ch}(x) - V_{TH}\right]$$

$$I_D = -WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right]v$$

Derivation of I/V Characteristics





$$I_D = -WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right]v$$

$$v = \mu E$$

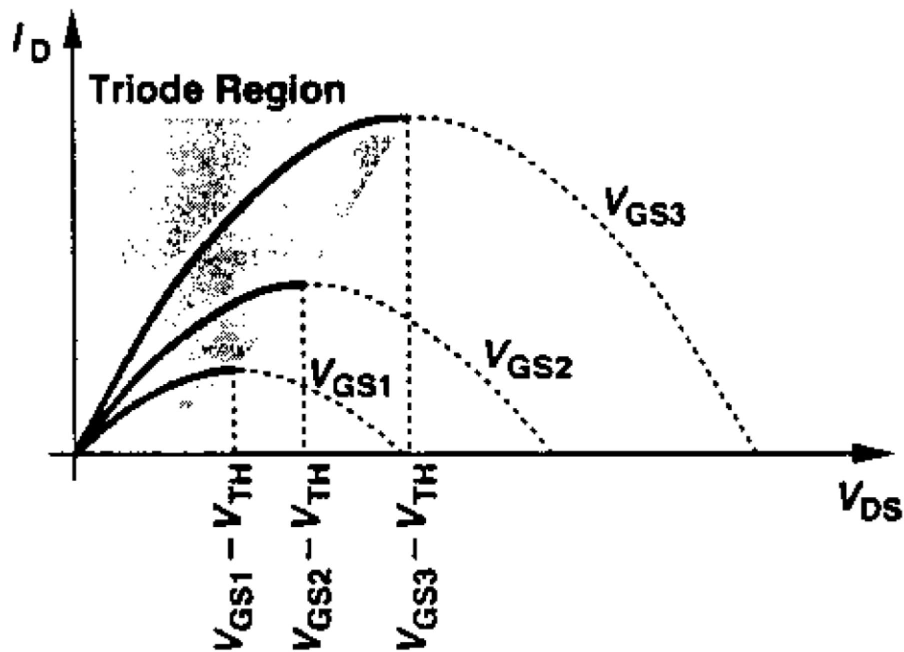
$$E(x) = -dV/dx$$

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}$$

$$V(0) = 0 \quad V(L) = V_{DS}$$

$$\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} WC_{ox}\mu_n[V_{GS} - V(x) - V_{TH}]dV$$

Since I_D is constant along the channel ➔ $I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$



$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$V_{GS} - V_{TH} \equiv \textit{overdrive voltage} \equiv \textit{effective voltage}$$

$$\frac{W}{L} \equiv \textit{aspect ratio}$$

$$\textit{if} \quad V_{GS} > V_{TH}\ , V_{GD} > V_{TH} \equiv V_{DS} < V_{GS} - V_{TH} \rightarrow \quad \textit{triode region}$$

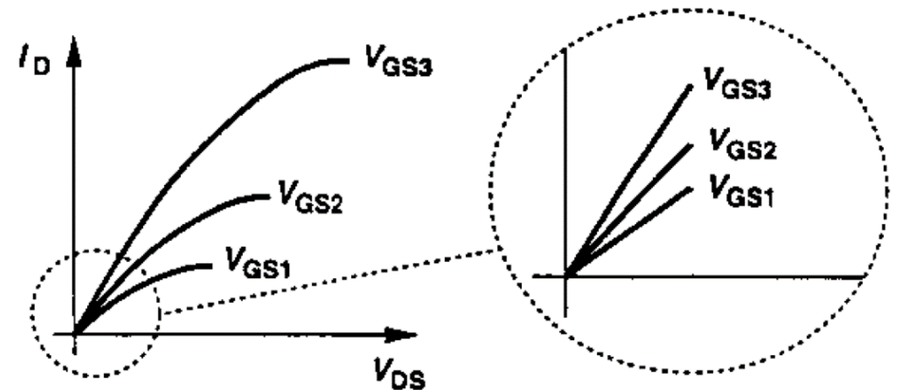
$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$if \quad V_{DS} << 2(V_{GS} - V_{TH}) \rightarrow \quad deep\ triode\ region$$

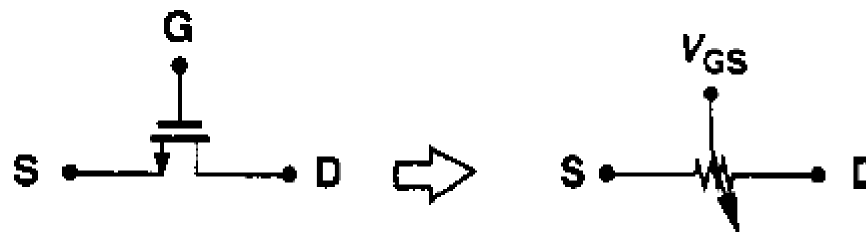
So we have:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}.$$

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}.$$

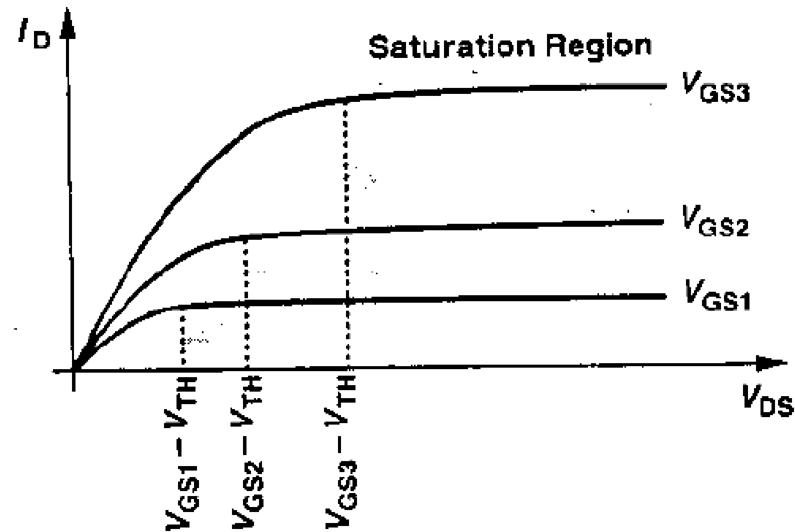


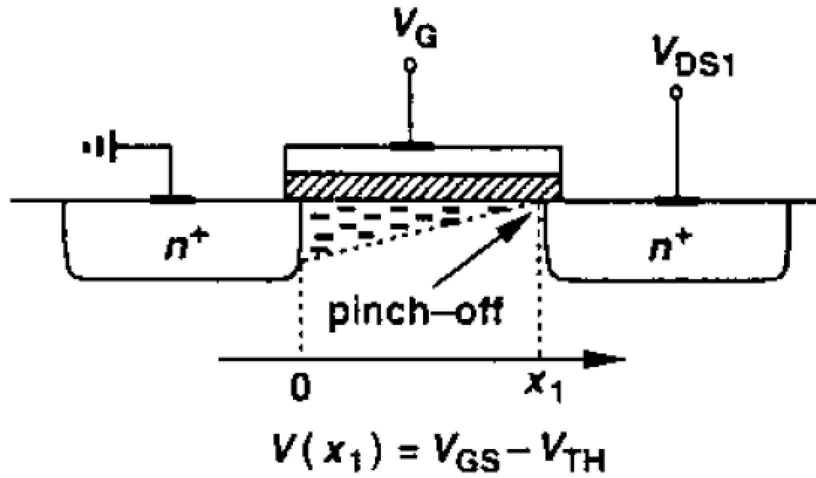
Linear operation in deep triode region

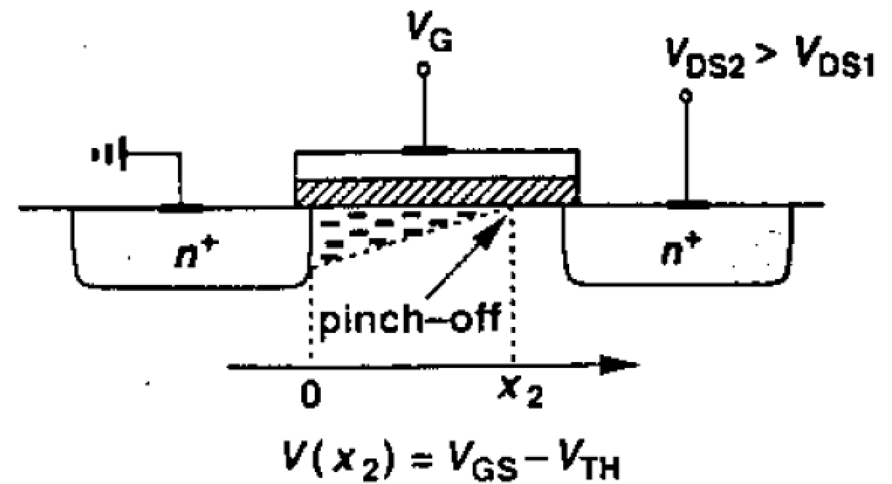


MOSFET as a controlled linear resistor

Saturation of the Drain Current

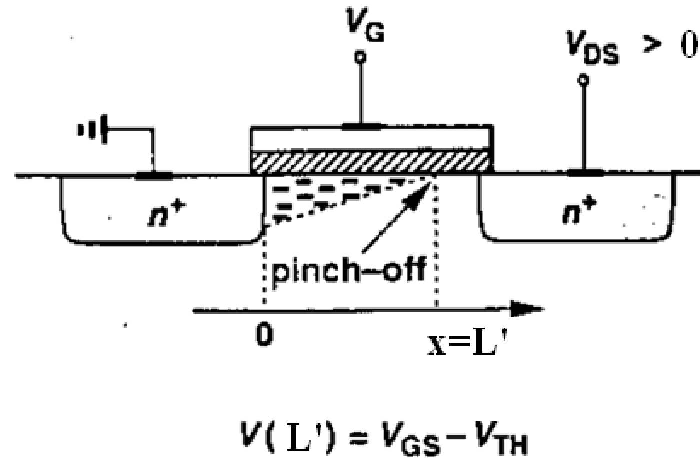






Pinch-off Behavior

Saturation of the Drain Current



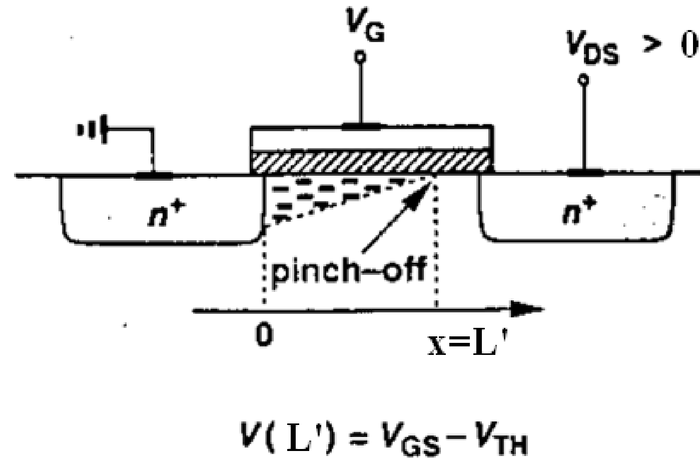
$$\int_{x=0}^{L'} I_D\,dx = \int_{V=0}^{V_{GS}-V_{TH}} W C_{OX} \mu_n \left[V_{GS} - V(x) - V_{TH}\right] dV$$

$x = 0$ to $x = L'$, where L' is the point at which Q_d drops to zero.

$V(x) = 0$ to $V(x) = V_{GS} - V_{TH}$

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2$$

Saturation Region



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$$

For long channel transistor, we have: $L \cong L'$

So the above formula is simplified as follows:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

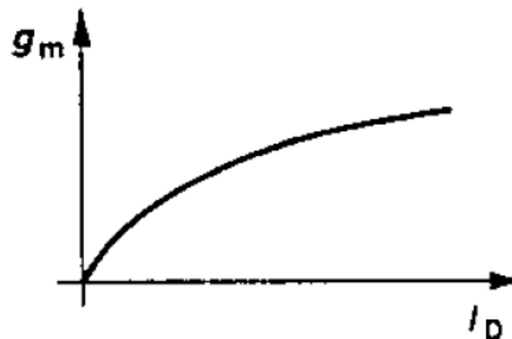
Transconductance of MOSFET

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

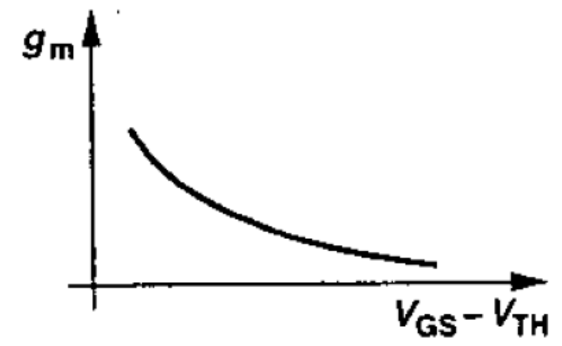
$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}.\text{const.}}$$

$$= \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$$

W/L Constant

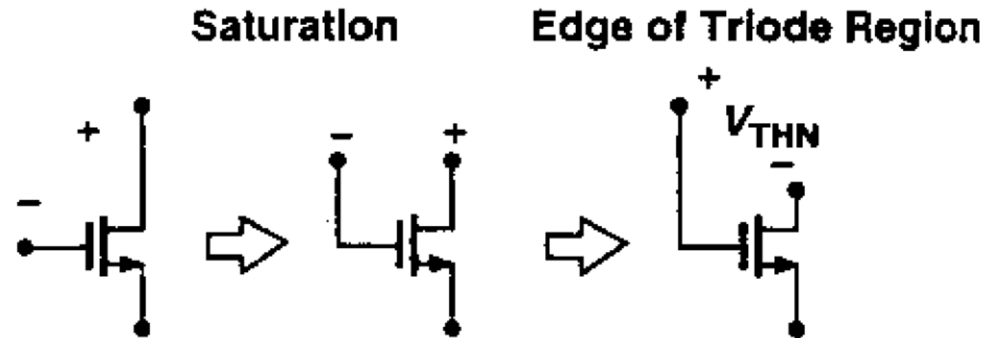


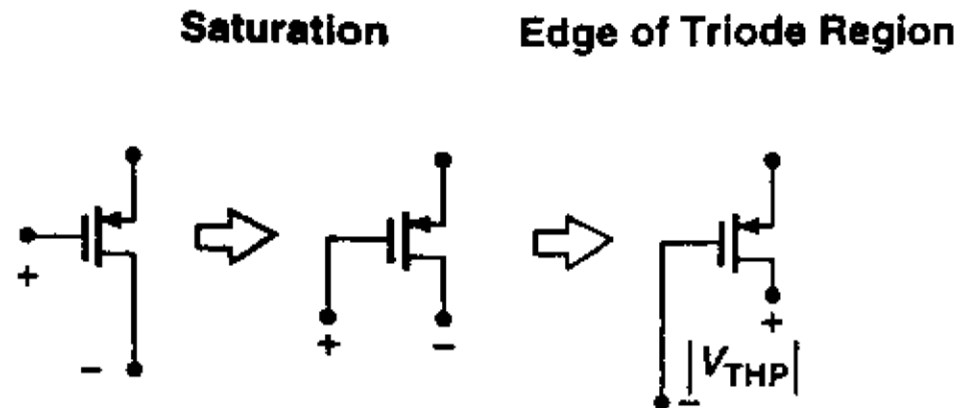
W/L Constant



I_D Constant

Conceptual Visualization of Saturation and Triode Regions





Second Order Effects

- **Body Effect**
- Channel-Length Modulation
- Subthreshold conduction
- Leakage current
- Short-channel effects

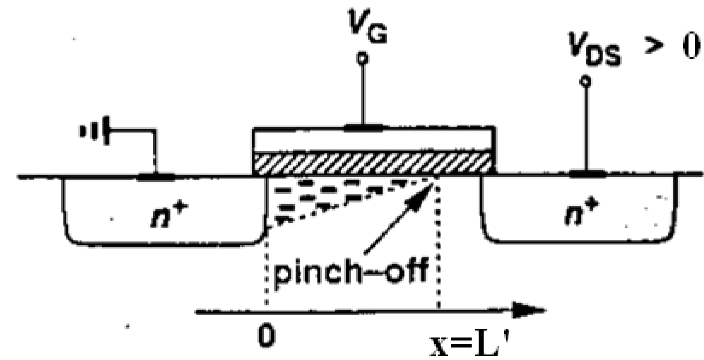
If $V_{SB}>0$ ➔ the threshold voltage V_{TH} is increased as follows:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$$

$$\gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$$

Second Order Effects

- Body Effect
- **Channel-Length Modulation**
- Subthreshold conduction
- Leakage current
- Short-channel effects



The actual length of the inverted channel gradually decreases as the value of V_D increases. In other words, L' is in fact a function of V_{DS}

$$L' = L - \Delta L$$

$$1/L' \approx (1 + \Delta L/L)/L$$

$$\Delta L/L = \lambda V_{DS}$$

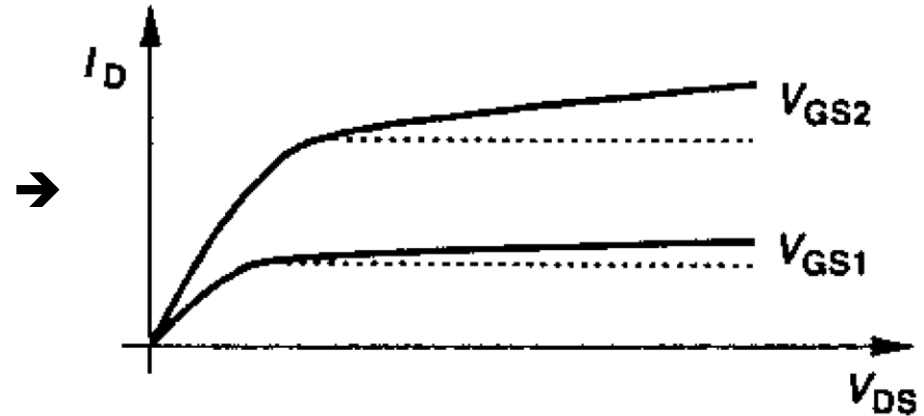
(from semiconductor devices course)

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$$

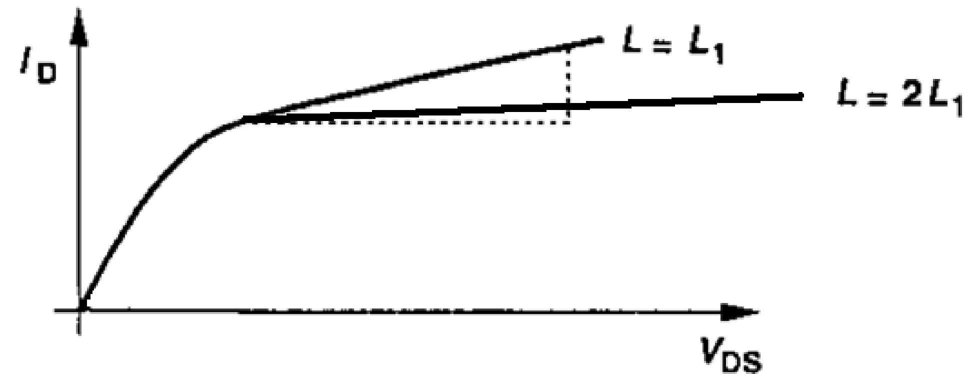
$$\Rightarrow I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

Second Order Effects

Channel-length modulation results in a nonzero slop in the I_D /V_{DS} characteristic. ➔



$$\frac{\Delta L}{L} = \lambda V_{DS} \quad \rightarrow \quad \lambda \propto \frac{1}{L}$$

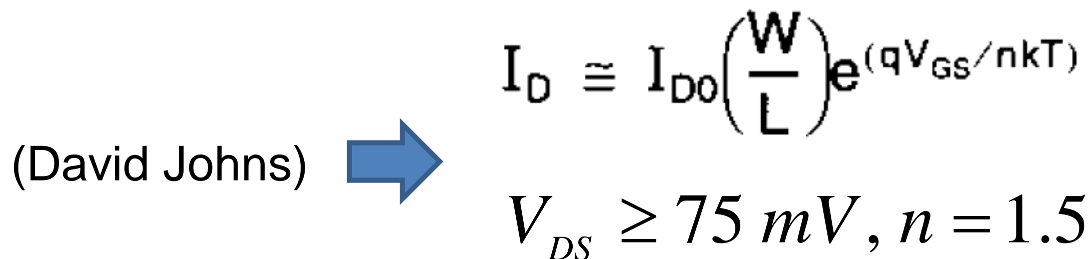


Therefore, for longer channels, λ is smaller.

Second Order Effects

- Body Effect
- Channel-Length Modulation
- **Subthreshold conduction**
- Leakage current
- Short-channel effects

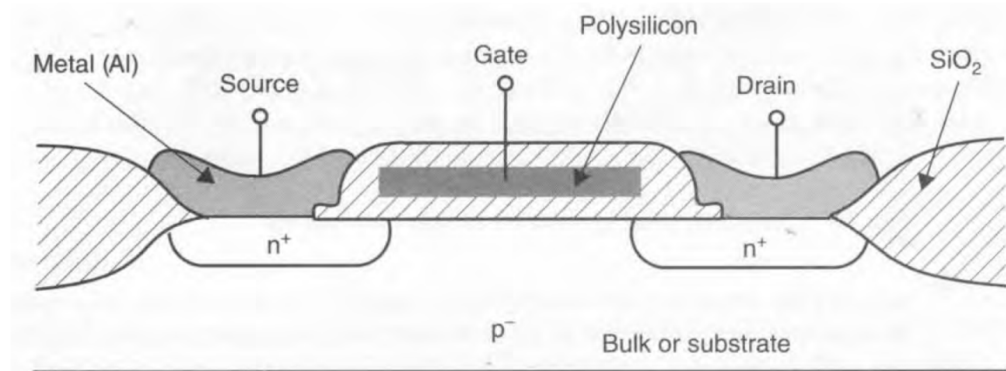
In reality, for $V_{GS}<V_{TH}$ a weak inversion layer still exist and some current flows from D to S. This phenomena is called weak inversion or subthreshold conductance.



Second Order Effects

- Body Effect
- Channel-Length Modulation
- Subthreshold conduction
- **Leakage current**
- Short-channel effects

The Leakage current of the PN junctions is important in estimating the maximum time a sample-and-hold circuit or a dynamic memory cell can be left in hold mode.
The leakage current doubles for every 11 °C rise in temperature.



Second Order Effects

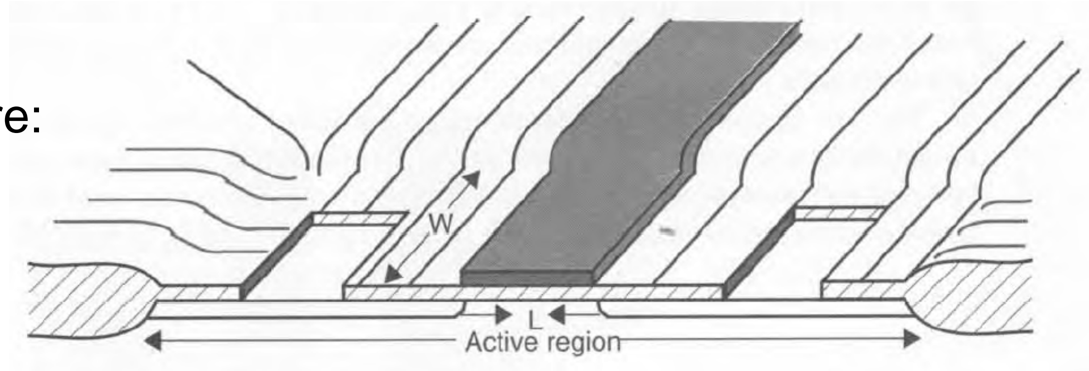
- Body Effect
- Channel-Length Modulation
- Subthreshold conduction
- Leakage current
- **Short-channel effects**

This phenomena will be discussed later (chapter 17, Razavi).

MOS Device Layout

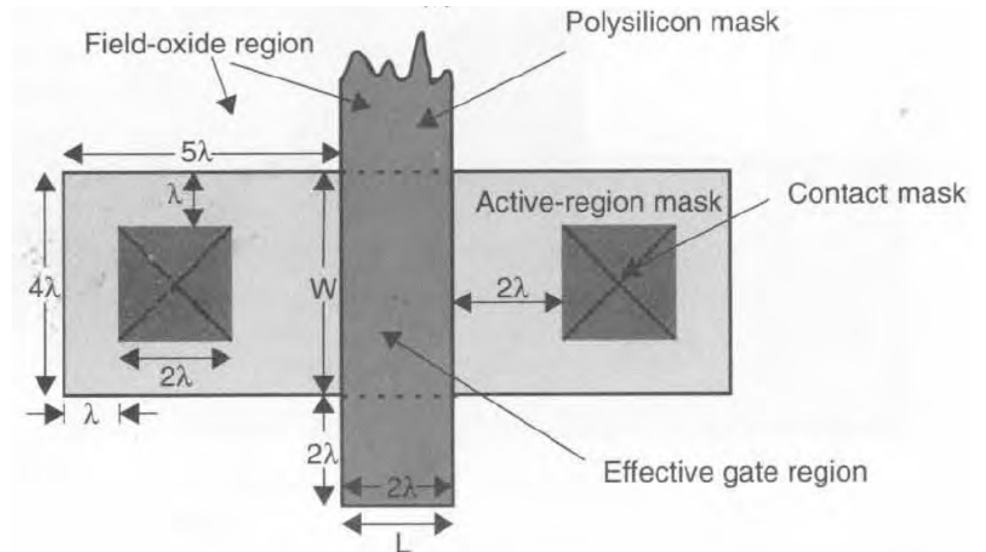
The two most important masks are:

- Active region mask
- Gate polysilicon mask

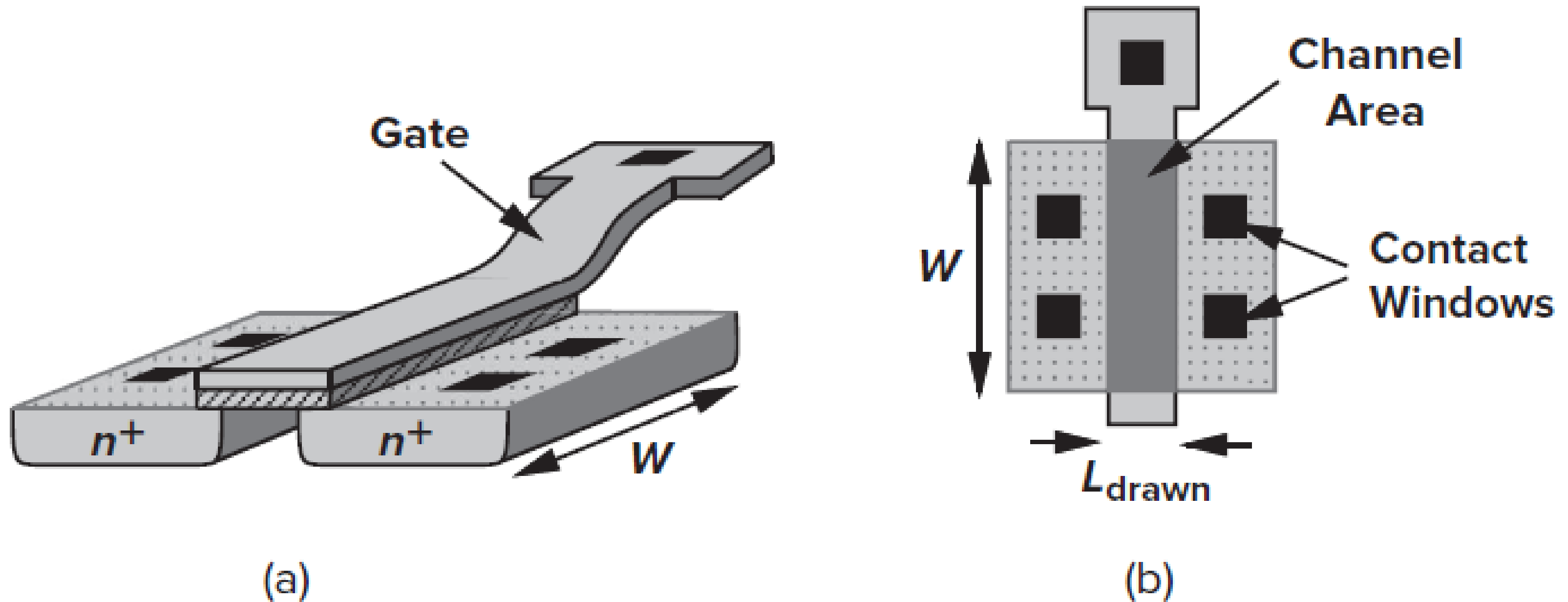


The intersection of these two masks becomes the channel region of the MOS transistor.

The design rules for laying out transistors are often expressed in terms of λ where λ is ½ the gate length.



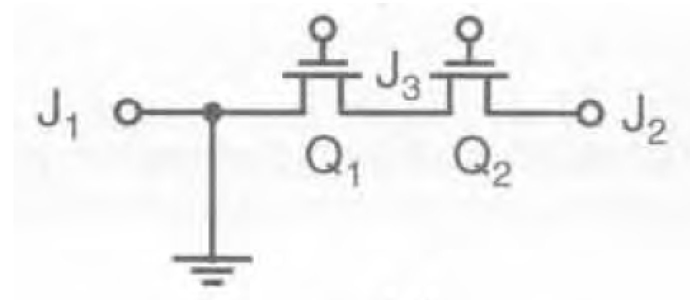
MOS Device Layout



When we are drawing the layout of a circuit, we must perform both the DRC and LVS tests.
DRC ➔ Design Rule Check
LVS➔ Layout Versus Schematic

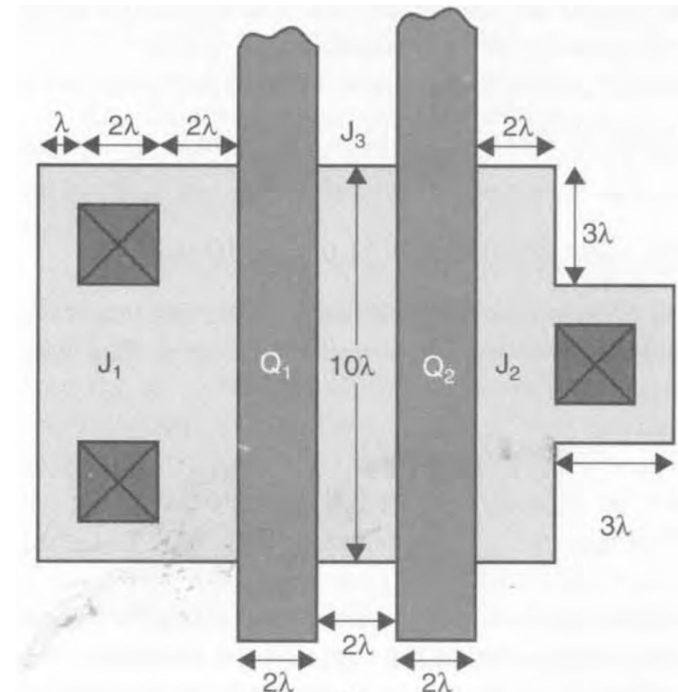
MOS Device Layout

Example:



Area: $A_{J1} = 5\lambda \times W$

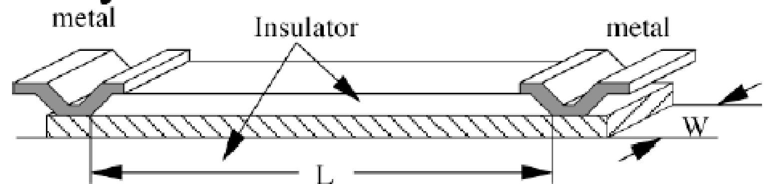
Peripheral: $P_s = 10\lambda + 2W$



Integrated Resistors

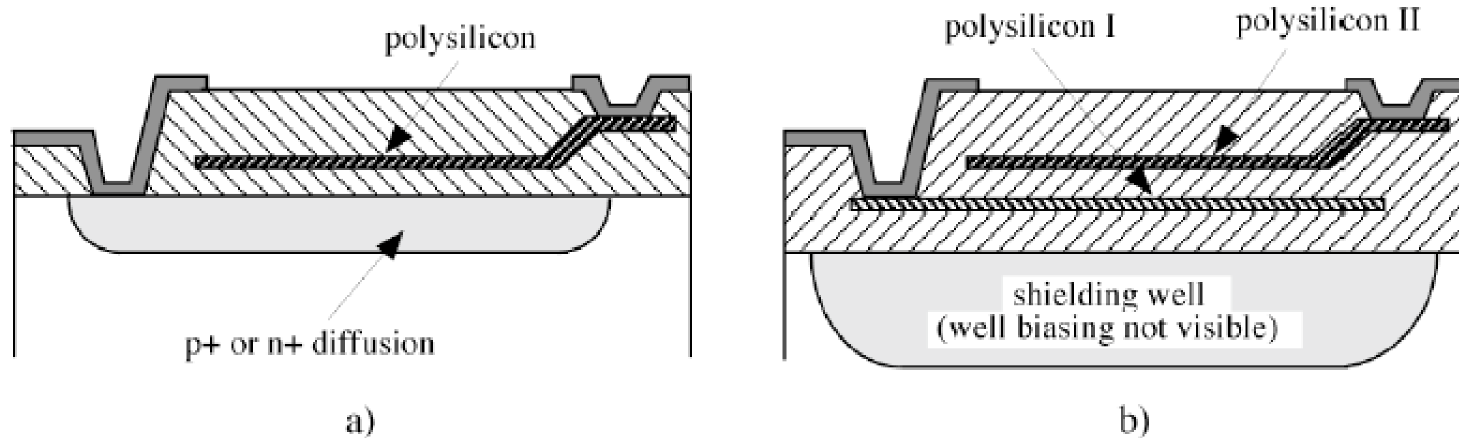
A resistor is a strip of resistive layer.

$$R = 2R_{cont} + \frac{L}{W} R_{\square}$$



Type of layer	Sheet resistance	Accuracy	Temperature coefficient	Voltage coefficient
	Ω/□	%	ppm/°C	ppm/V
n^+ diff	30-50	20-40	200-1K	50-300
p^+ diff	50-150	20-40	200-1K	50-300
n-well	2K-4K	15-30	5K	10K
p-well	3K-6K	15-30	5K	10K
pinched n-well	6K-10K	25-40	10K	20K
pinched p-well	9K-13K	25-40	10K	20K
poly 1	20-40	25-40	500-1500	20-200
poly 2	15-40	25-40	500-1500	20-200

Types of integrated capacitors

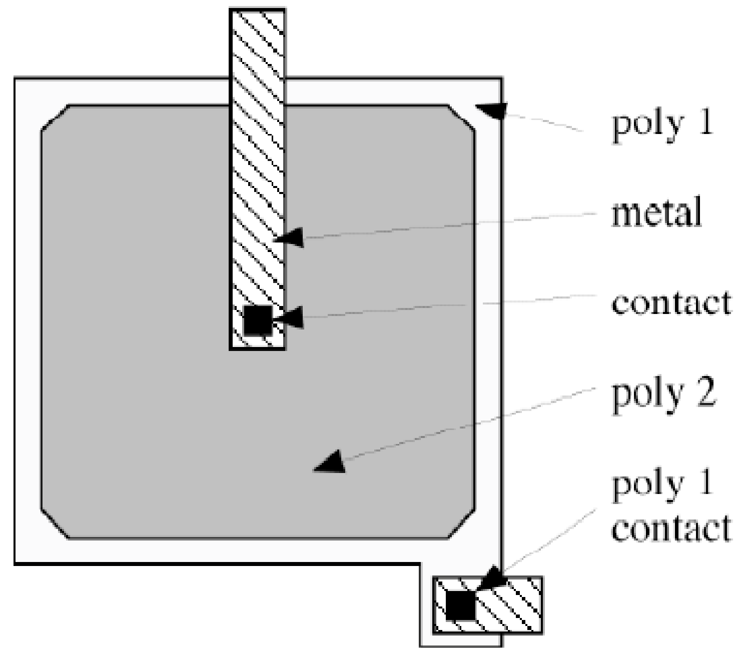


Electrodes: metal; polysilicon; diffusion
Insulator: silicon oxide; polysilicon oxide; CVD oxide

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

$$\left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2$$

Integrated capacitors



To achieve good matching:

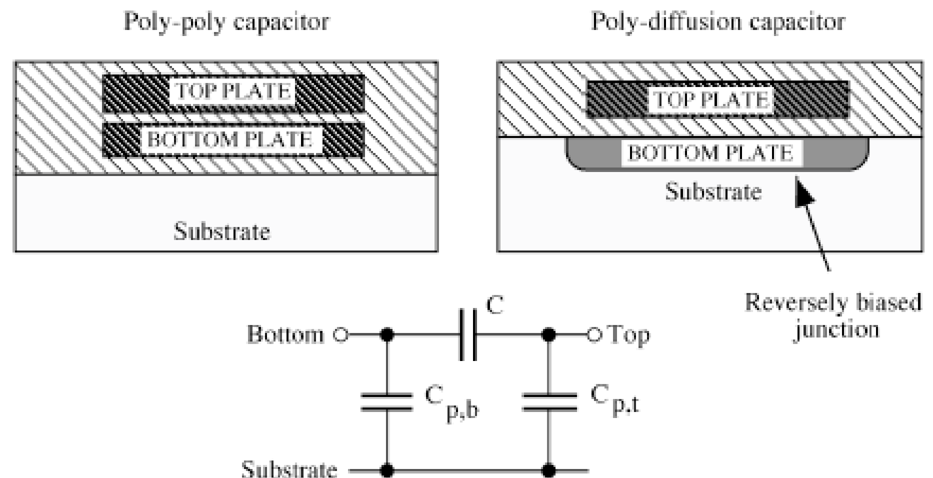
- Use of unity capacitors connected in parallel.
- Use $W = L$ fairly large.

Capacitors Features

Type	t_{ox}	Accuracy	Temperature coefficient	Voltage coefficient
	nm	%	ppm/°C	ppm/V
poly-diff	6-20	7-14	20-50	60-300
poly1-poly2	8-25	6-12	20-50	40-200
metal-poly	500-700	6-12	50-100	40-200
metal-diff	1200-1400	6-12	50-100	60-300
metal1-metal2	800-1200	6-12	50-100	40-200

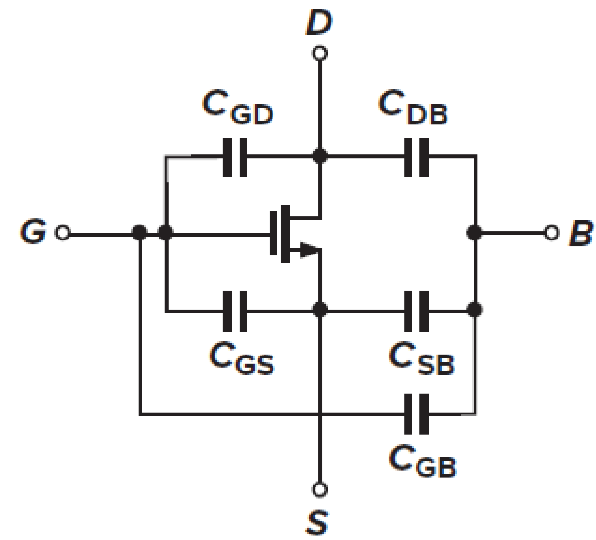
Parasitic capacitances:

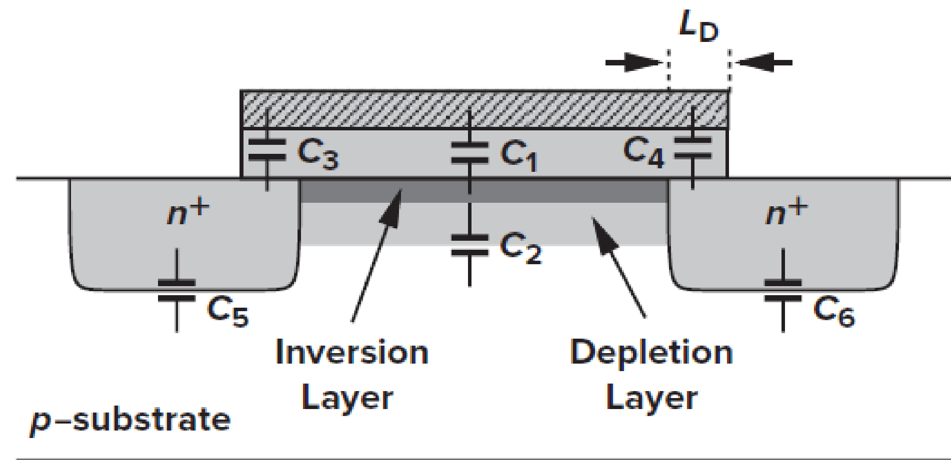
	diffusion	poly-poly or poly-metal
$C_{p,b}$	$0.1\ C$	$0.01\ C$
$C_{p,t}$	$0.01\ C$	$0.001\ C$



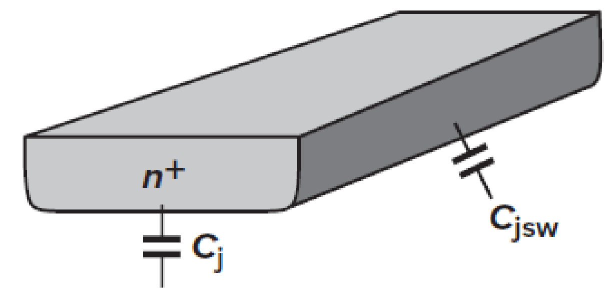
MOS Device Capacitances

C1 or C_{ch}: oxide capacitance
C2 or Cd: depletion capacitance
C3,C4: overlap capacitance
C5,C6: junction capacitance



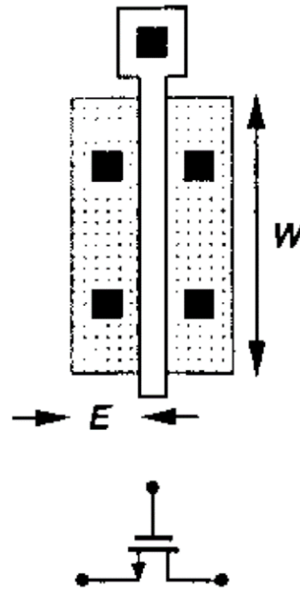


(a)



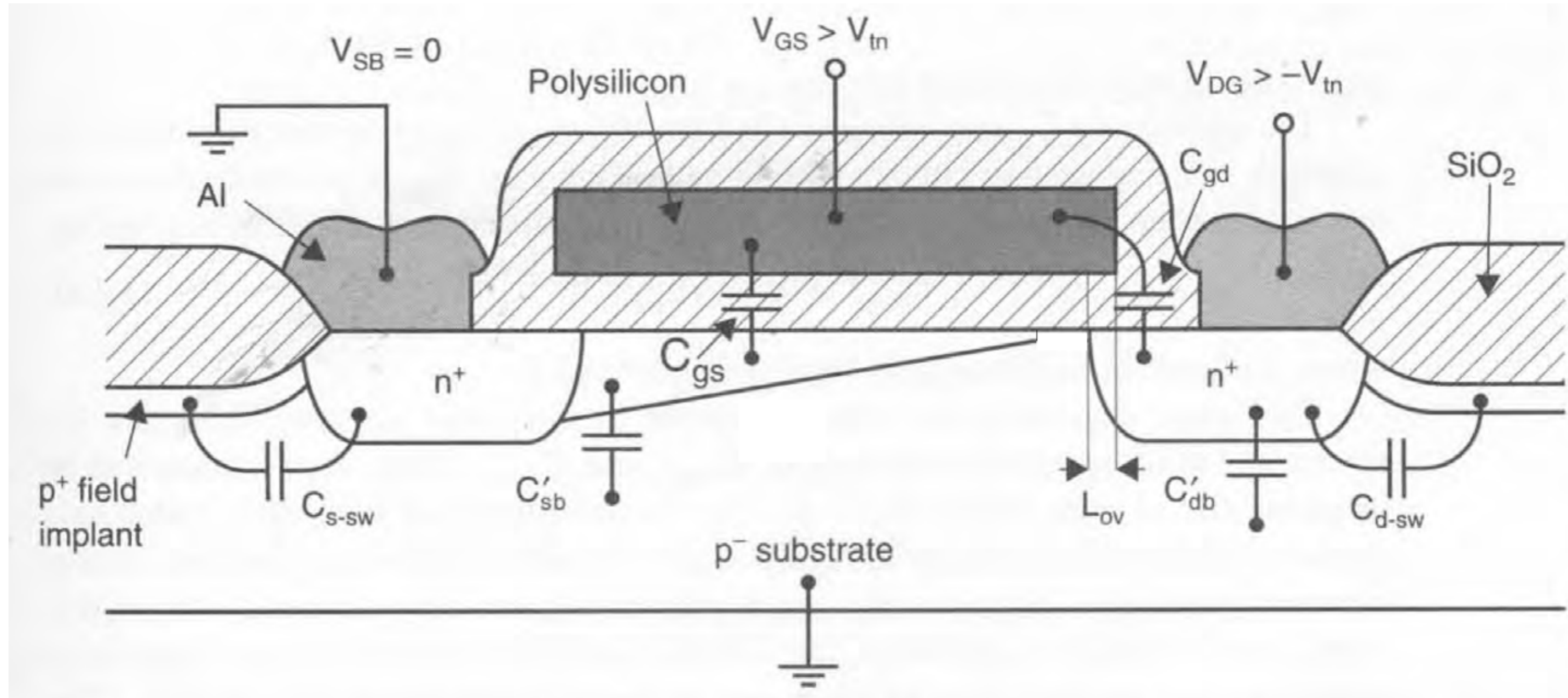
(b)

Effect of Layout on Parasitic Capacitances



$$C_{DB} = C_{SB} = (W \times E)C_j + 2(W + E)C_{jsw}$$

MOS Device Capacitances (Saturation Region)



MOS Device Capacitances (Saturation Region)

$$C_{GS} = \frac{2}{3}WL_{eff}C_{ox} + WC_{ov} \cong \frac{2}{3}WLC_{ox}$$

$$C_{GD} = WC_{ov} \cong WL_D C_{ox}$$

$C_{GB} \cong 0$ C_{GB} is neglected because inversion layer act as a shield.

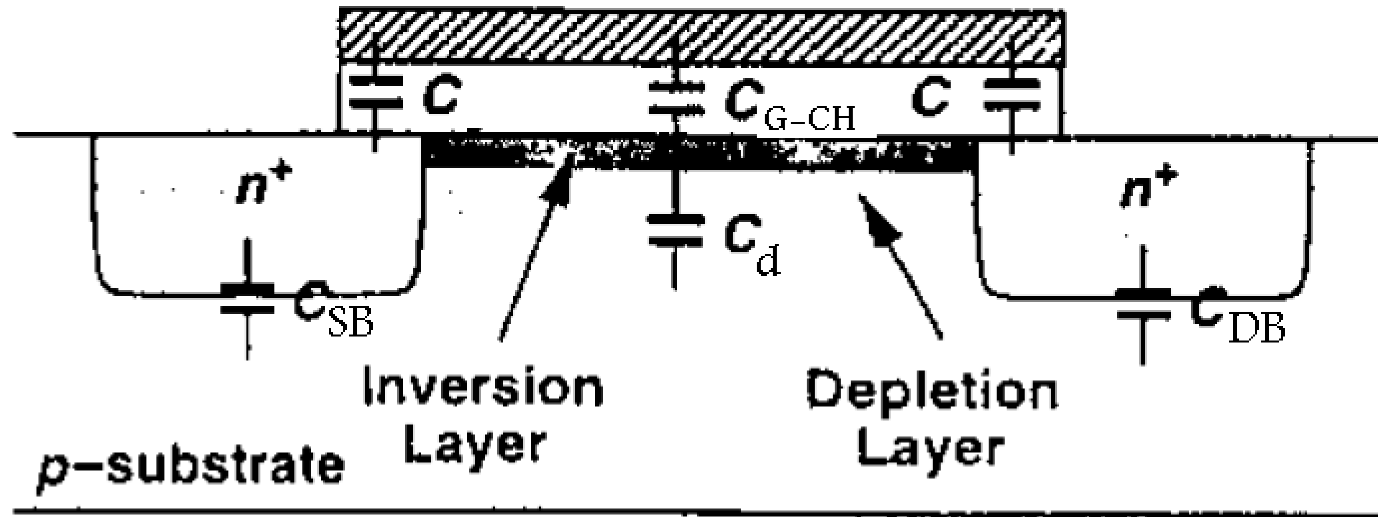
$$C_{SB} = \left(A_s + A_{ch}\right)C_j + P_s C_{jsw}, \quad A_{ch} = WL_{eff}$$

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_{SB}}{\varphi_B}\right)^m}, C_{jsw} = \frac{C_{jsw-0}}{\left(1 + \frac{V_{SB}}{\varphi_B}\right)^m} 0.3 \le m \le 0.4, \varphi_B : built-in\ voltage$$

$$A_s : source\ area \quad P_s : source\ perimeter$$

$$C_{DB} = A_d C_j + P_d C_{jsw}, C_j = \frac{C_{j0}}{\left(1 + \frac{V_{DB}}{\varphi_B}\right)^m}, C_{jsw} = \frac{C_{jsw-0}}{\left(1 + \frac{V_{DB}}{\varphi_B}\right)^m}$$

MOS Device Capacitances (Deep Triode Region)



$C = WC_{ov}$

$C_{G-CH} = WLC_{ox}$

MOS Device Capacitances (Deep Triode Region)

$$C_{GS} \cong \frac{WLC_{ox}}{2} + WC_{ov}$$

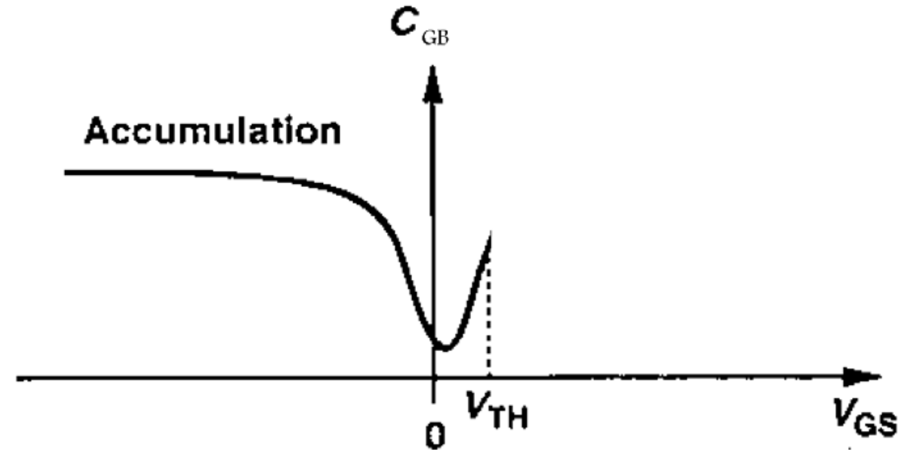
$$C_{GD} \cong \frac{WLC_{ox}}{2} + WC_{ov}$$

$C_{GB} \cong 0$ C_{GB} is neglected because inversion layer act as a shield.

$$C_{SB} = \left(A_s + \frac{A_{ch}}{2}\right)C_j + P_s C_{jsw},\ C_j = \frac{C_{j0}}{\left(1 + \frac{V_{SB}}{\varphi_B}\right)^m},\ C_{jsw} = \frac{C_{jsw-0}}{\left(1 + \frac{V_{SB}}{\varphi_B}\right)^m}$$

$$C_{DB} = \left(A_d + \frac{A_{ch}}{2}\right)C_j + P_d C_{jsw},\ C_j = \frac{C_{j0}}{\left(1 + \frac{V_{DB}}{\varphi_B}\right)^m},\ C_{jsw} = \frac{C_{jsw-0}}{\left(1 + \frac{V_{DB}}{\varphi_B}\right)^m}$$

MOS Device Capacitances (Cut-off)



$$C_{GS} = WC_{ov}$$

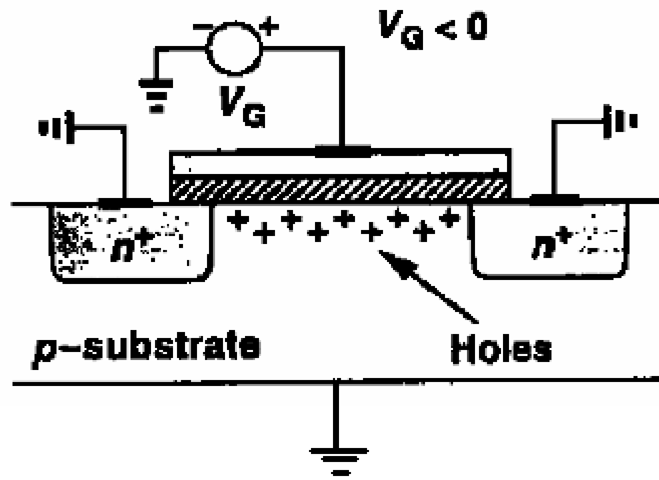
$$C_{GD} = WC_{ov}$$

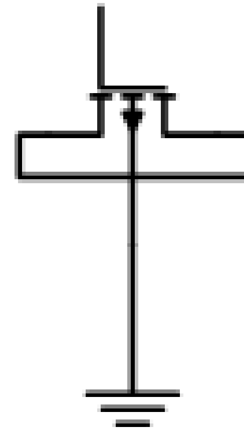
$$C_{GB} \cong \frac{C_d (WLC_{ox})}{C_d + (WLC_{ox})}, C_d : \text{depletion capacitance}, \quad \text{if } V_G << 0 \Rightarrow C_{GB} \cong WLC_{ox}$$

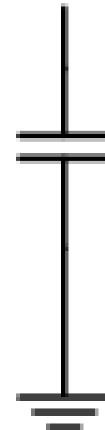
$$C_{SB} = A_s C_j + P_s C_{jsw}, C_j = \frac{C_{j0}}{\left(1 + \frac{V_{SB}}{\varphi_B}\right)^m}$$

$$C_{DB} = A_d C_j + P_d C_{jsw}, C_j = \frac{C_{j0}}{\left(1 + \frac{V_{DB}}{\varphi_B}\right)^m}$$

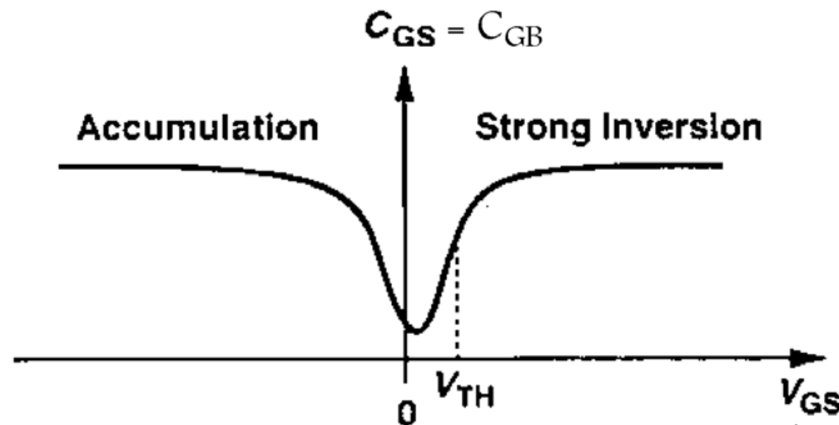
Beahvior of MOS Device as a Capacitor





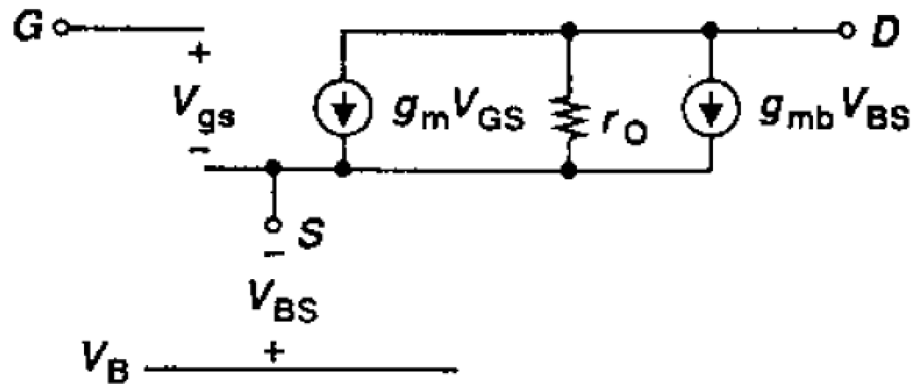


NMOS operating in accumulation region



MOS Low-Frequency Small-Signal Model

(active region)



$$r_O = \frac{\partial V_{DS}}{\partial I_D} \approx \frac{1}{\lambda I_D}$$

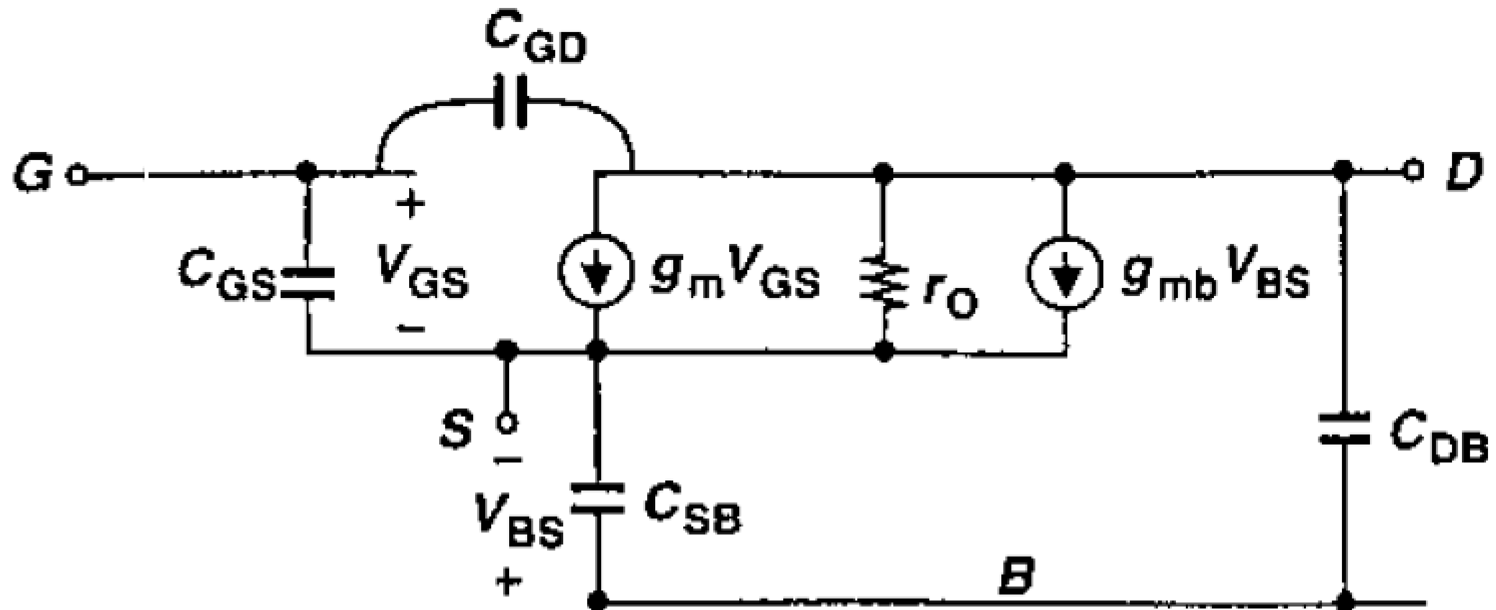
$$\lambda \propto \frac{1}{2L\sqrt{V_{DS} - V_{eff} + \Phi_B}}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})\left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right).$$

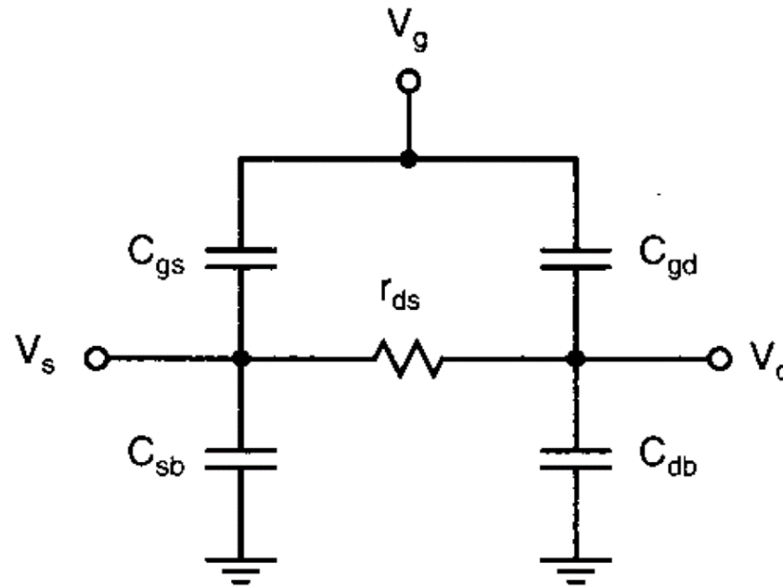
$$\frac{\partial V_{TH}}{\partial V_{BS}} = -\frac{\partial V_{TH}}{\partial V_{SB}} = -\frac{\gamma}{2}(2\Phi_F + V_{SB})^{-1/2}.$$

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta g_m,$$

MOS Small-Signal Model
(active region)

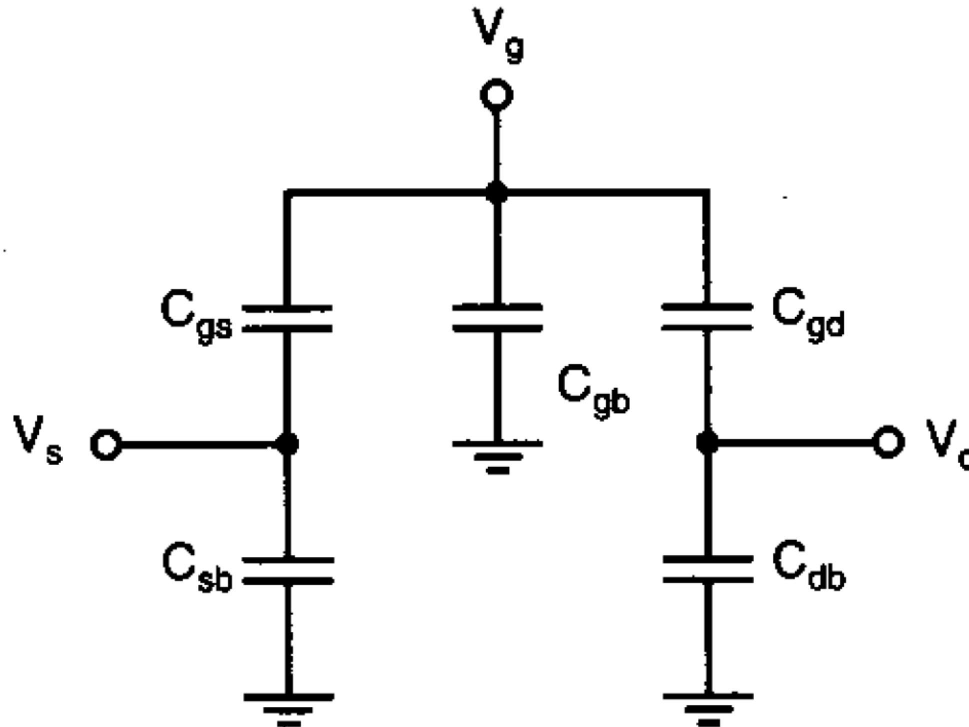


MOS Small-Signal Model (triode region)



$$r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right)}$$

MOS Small-Signal Model
(Turn off region)



MOS SPICE Model

Level 1 SPICE models for NMOS and PMOS devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

0.5 μm CMOS Technology

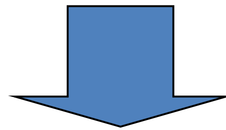
MOS SPICE Model

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body-effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate-oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

Comparison between NMOS and PMOS

PMOS devices are quite inferior to NMOS transistors.

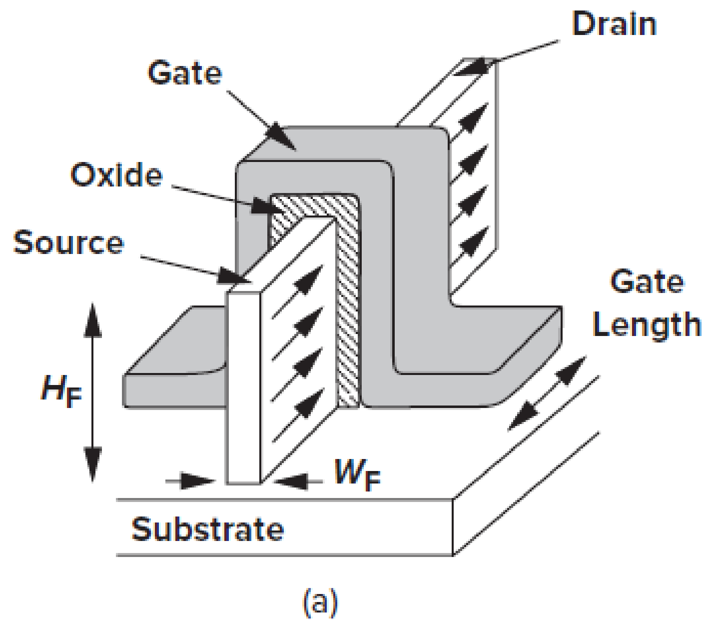
For example, due to the lower mobility of holes: $\mu_p C_{ox} \cong 0.5 \mu_n C_{ox}$



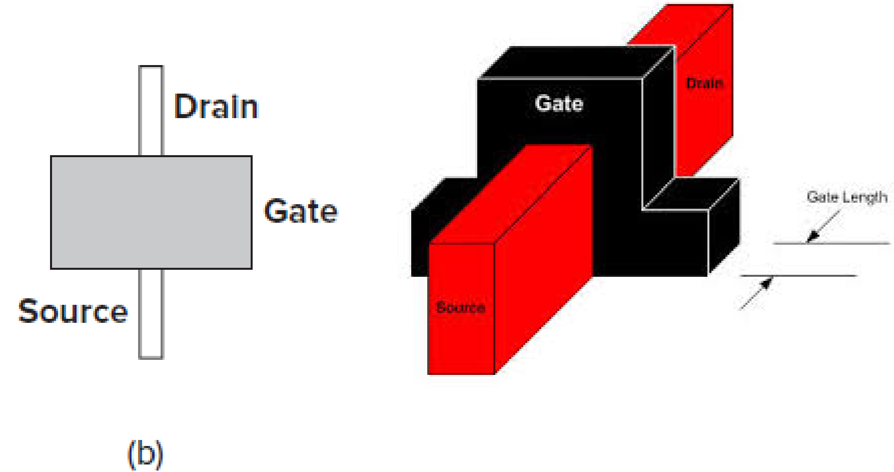
$$g_{m_p} < g_{m_n}$$

Besides, for a given current and dimension we have: $r_{o_p} < r_{o_n}$

FinFET



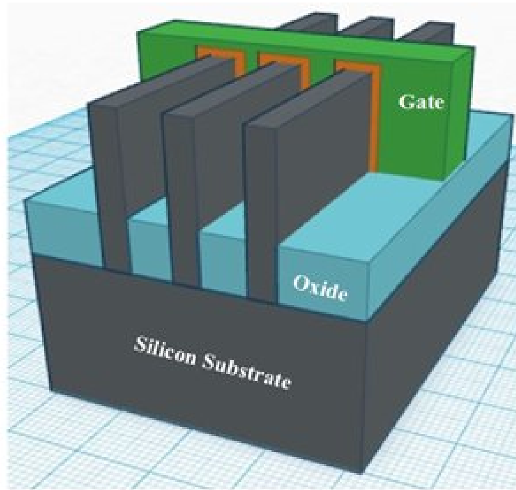
(a)

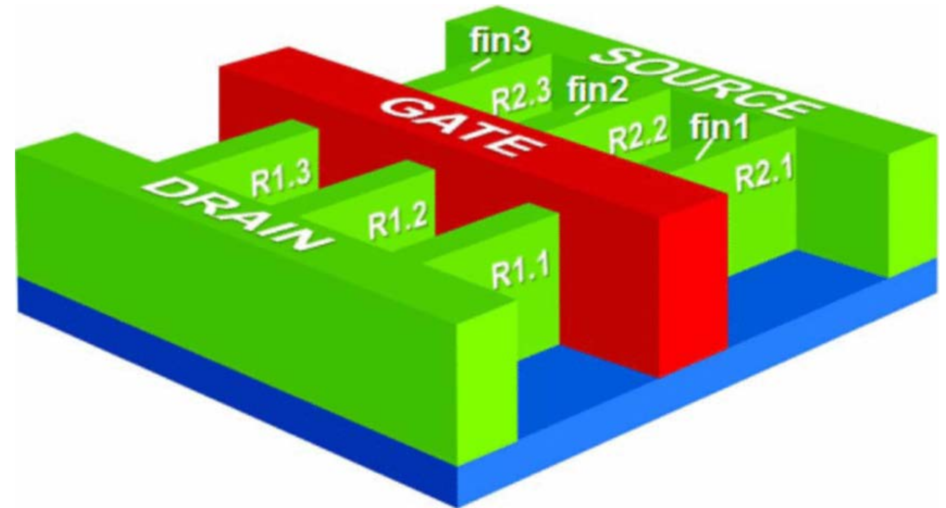


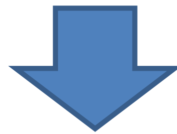
(b)

- FinFET utilizes a three-dimensional structure, which results in small channel length about 20nm.
- Equivalent channel width: $W = W_F + 2H_F$
- Typically, W_F=6nm, H_F=50nm.
- In practice, the designer does not have any control on W_F and H_F.
- Wider transistors can be obtained by increasing the number of fins.

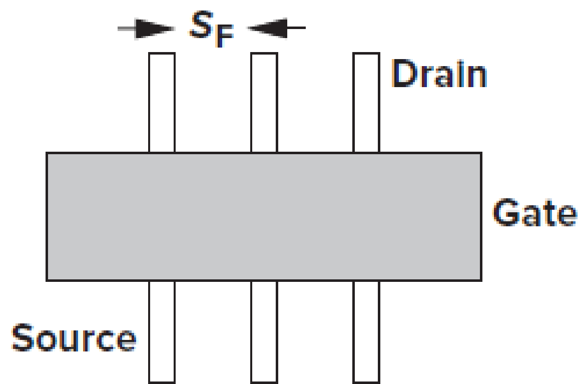
Utilizing Multiple Fins

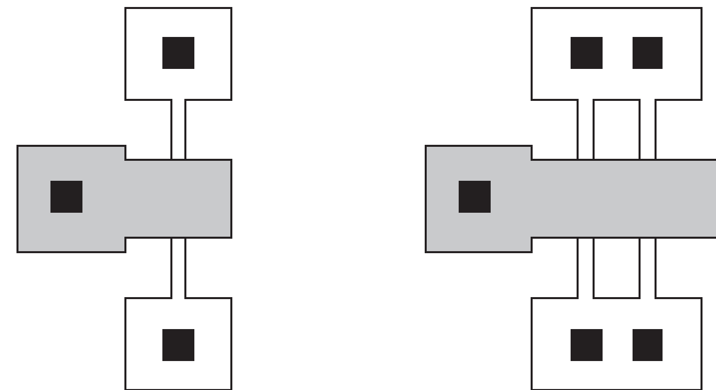






Top View





Layout of single- and double-fin transistors.