# Low Power High Speed Dynamic Comparator

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***Abstract*—In this study, we proposed a novel technique to enhance the performance of the dynamic comparator. The pre-amplifier outputs are directly connected to the latching nodes through switches that are controlled by output logics. Hence, the path of static current will be disconnected after making decision. Comparing to the previous dynamic comparators, the proposed structure shows significant performance improvement. The comparator has been simulated in standard 90nm technology. Simulation results show that the proposed comparator is suitable for low power, high speed applications.**

***Keywords*—Dynamic comparator, High speed analog to digital converters, low power, scaled CMOS technology.**

## I. Introduction

High speed low power comparators are necessary in todays high performance analog-to-digital converters (ADCs). Designing high speed comparators becomes challenging in the scaled CMOS technology, since supply and threshold voltages of devices are not scaled with same factor. The fast speed and low power consumption of the dynamic comparators make them suitable for high speed ADCs.

Latch type voltage sense amplifier is popular due to its high input impedance, full swing output and absence of static power consumption [1]. However, due to the several stacked transistors, a high voltage headroom is required for it to operate properly, which is challenging in the scaled CMOS technology. The speed and offset of this structure is highly sensitive to input common mode voltage [1], which is not appropriate for application with input common mode variations.

Double tail comparator, has less stacking transistors, which makes it suitable for low voltage applications. Amplification and latch stages are separated from each other, which enables it to employ low tail current in the former and high current in the latter, leading to low offset and high speed respectively [1]. However, the tail current of amplification stage depends on the input common mode voltage, causing sensitivity of the comparator offset to the input common mode voltage.

The faster comparator is presented in [2]. In this structure the comparator output is connected directly to the latching nodes. However, the existence of static power in the amplification phase [3] makes it inappropriate for low power applications. An alternative solution is presented [4], which controls the tail transistor of pre-amplifier by logic gates and avoids static power consumption in the latching phase. However, still a hidden static current path exists in the latching phase, which significantly impacts the power and speed of comparator.

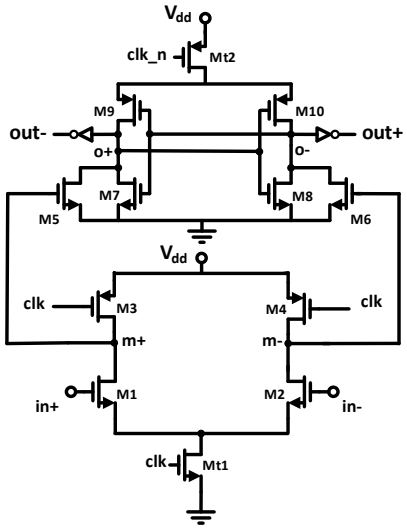


Fig. 1. Conventional double tail comparator

In this paper, we present a technique to reducing the power consumption of dynamic comparator. The proposed comparator fully benefits from direct connection of amplification stage to latching nodes for speed improvement without increasing the power consumption. Simulation results show that its offset and power consumption have less sensitivity to input common mode variation.

This paper is organized as follows. Section II briefly reviews previous works on dynamic comparators. Proposed structure is introduced in section III. Simulation results are provided in section IV, and finally section V contains the conclusion of the whole study.

## II. Conventional Dynamic Comparators

Conventional double tail comparator is shown in Fig. 1 This structure is composed of amplification and latch stages with fewer stacked transistors, which enables it to be employed in the low voltage applications. It is also possible to employ low tail current in the amplification stage to enhance the offset of

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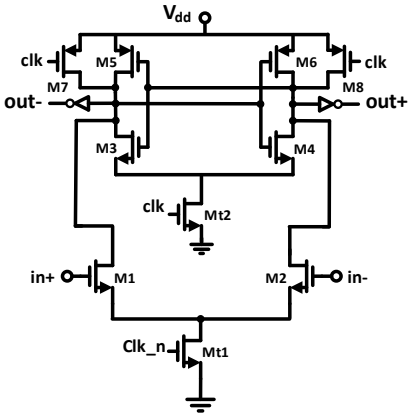


Fig. 2. Comparator presented in [2]

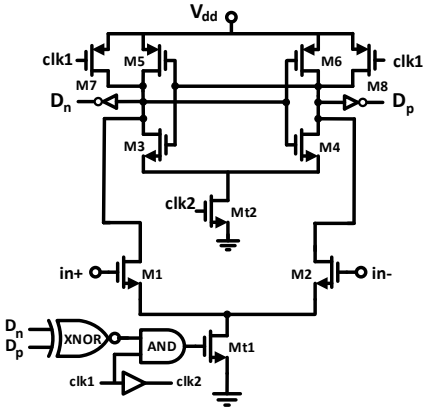


Fig. 3. Comparator presented in [4]

the comparator. In addition, the current in the latching stage can be increased for faster regeneration.

The operation of the comparator, shown in Fig. 1, is as follows. During reset phase, $clk = 0$, and both $Mt1$ and $Mt2$ are kept off. $M3$ and $M4$ are switched on and the drain voltage pulled up to $V_{dd}$. Also, $M5$ and $M6$ pull the latching nodes down to the ground. When clock goes high (latching phase, $clk = V_{dd}$), tail transistors ($Mt1$ and $Mt2$) will be turned on. In this phase input transistors ($M1$ and $M2$) will pull down their drain voltages with different rates, regarding to the input differential voltage. Also, $M5$ and $M6$ provide voltage amplification to the latching nodes. At the beginning of the latching phase, $M9$ and $M10$ will be turned on and pull up the latching node until one of the nmos pairs ($M7$ or $M8$) is turned on. Finally, the latch will regenerate the voltage difference.

However, the current of $Mt1$ is dependent on the input common mode voltage, causing sensitivity of the comparator offset to the input common mode voltage. Hence, this structure is not appropriate for SAR ADCs with energy efficient switching schemes like monotonic or set-and-down schemes, since it will degrade their linearity.

The comparator in [2] is shown in Fig. 2. This comparator is composed of preamplifier and latch stages. In the amplification phase ($clk = 0$) $Mt1$ is turned on, $M1$ and $M2$ amplifies the input difference, also $M7$ and $M8$ are turned on and act as a resistive loads. So, the initial voltage for the latching phase is provided in this phase. In the latching phase ($clk = V_{dd}$), $Mt1$, $M7 - 8$ will be turned off and $Mt2$ will be turned on and the back to back inverter composed of $M3 - 6$ will start regeneration.

In this structure, pre-amplifier outputs are directly connected to the latching nodes to reduce the overall delay. However, the load capacitance at the latching nodes increases [3], which in turn slows down the speed of comparator. In addition, the circuit has static power in the pre-amplification phase. Hence, this structure is not appropriate for low power applications.

A new comparator based on the structure [2] has been presented [4] as shown in Fig. 3. This structure employs one $XNOR$ and $AND$ gates to control the tail transistor of the pre-amplifier and avoid static power consumption in the latching phase. Also, $clk2$ is delayed signal of $clk1$, which can reduce the input-referred noise by maintaining $M1$ and $M2$ in the saturated state when $clk1$ is high voltage and $clk2$ is low voltage [4].

The operation of this structure is as follows. In the reset phase, $clk1$ and $clk2$ are low voltage and $Mt1$ and $Mt2$ are off. Also, $M7$ and $M8$ are on and pull up the latching nodes to $V_{dd}$. In the latching phase, $Mt1$ is turned on and $M1$ and $M2$ pull their drain voltages down with different rates. Also, regeneration will be started as soon as $clk2$ goes to high voltage.

When the decision is made, $Dn$ and $Dp$ will turn off $Mt1$ through $XNOR$ and $AND$ gates. Hence, it will avoid static power consumption through $Mt1$ in the latching phase.

On the other hand, the disadvantage of this structure is that again the pre-amplifier output is directly connected to the latching nodes, which increase the load capacitance and slow down the regeneration.

Another important drawback of this structure is that, there is a hidden static current path in the latching phase that will significantly degrade the speed and power consumption of this structure and overwhelm its advantages. This path is shown in Fig. 4. The gray transistors are turned off and static current path is shown by dashed line. Suppose $INp$ is higher than $INn$. Thus $O_n$ is discharged faster than $O_p$ and latch starts regeneration and try to pull $O_n$ and $O_p$ nodes down to the ground and up to $V_{dd}$, respectively. As soon as $O_n$ and $O_p$ reach the value that can change the output of inverters ($Dn$ and $Dp$), $Mt1$ is turned off by $Dn$ and $Dp$, through $XNOR$ and $AND$ gates. As seen in Fig. 4, $M6$ tries to pull up $O_p$ to $V_{dd}$ and $M2$ is charging its source voltage. Since $Mt2$ is on and $M3$ is trying to pull On down to the ground, the source of $M1$ reaches higher voltage compared to its drain terminal ($O_n$). Hence, the drain and source of $M1$ is replaced

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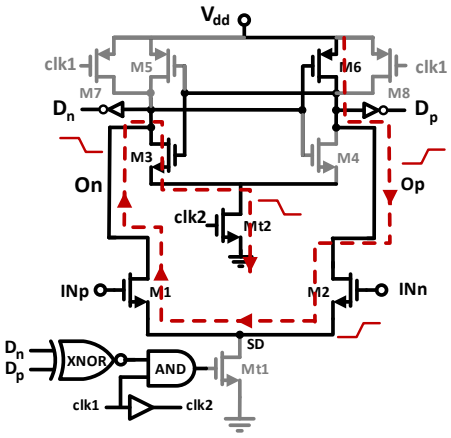


Fig. 4. Static current path (laching phase) in the comparator presented in [4]

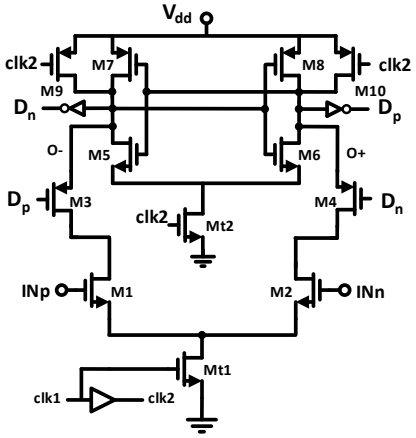


Fig. 5. Proposed dynamic comparator

with each other and static current flows through the path as shown in Fig. 4. This current will be increased for higher values of input common mode voltages, causing higher power consumption. Therefore, this structure is not appropriate for low power applications.

## III. Proposed Dynamic Comparator

Proposed dynamic comparator is shown in Fig. 5. $clk2$ denotes the delayed signal of $clk1$, which reduces the input-referred noise. This structure consists of pre-amplifier ($Mt1$, $M1$ and $M2$), two switches ($M3$ and $M4$) at the output of pre-amplifier and latch ($M5-10$). The operation of the comparator is as follows. In the reset phase, $clk1$ and $clk2$ become low, $Mt1$ and $Mt2$ are turned off and $M9$ and $M10$ charge the latching nodes to $V_{dd}$. Also, $M3$ and $M4$ are on and the drain of input transistors is pulled up to $V_{dd}$.

In the latching phase $M3$ and $M4$ are on and $Mt1$ will be turned on, hence input transistors will pull down the latching nodes by different speed with respect to the input differential voltage. As soon as $clk2$ goes to high, the regeneration will be started. After making the decision, comparator outputs will control the $M3$ and $M4$ switches to avoid static power consumption. Suppose $INp$ is higher than $INn$. Thus $O-$ drops faster than $O+$. After the decision is made, outputs will be changed to: $Dn = V_{dd}$ and $Dp = 0$. Hence, transistor $M4$ will be turned off to avoid static power consumption and $M3$ remains on to speed up the latch operation.

The advantages of the proposed structure are as follows:

1) The parasitic capacitors of the input transistors are not loading the latching nodes. Since input transistors are sized large enough to meet the offset requirements, their parasitic capacitance is large. Capacitive load of latch in the proposed structure decreases, which significantly improves the speed of regeneration.

2) The position of switches in the proposed comparator ensures that no static power will exist in the reset and latching phases.

3) Comparators presented in [2] and [4] try to connect pre-amplifier outputs directly to the latching nodes to speed up their regeneration. However, static power consumption in the amplification phase in [2], and latching phase in [4], overwhelm their advantages. The proposed structure takes the full advantages of the main idea without increasing power consumption.

## IV. Simulation Results

The performances of four comparators were compared by simulation. All comparators were designed with great care in same size input transistors in the standard 90nm CMOS technology. The results were measured at $1GHz$ frequency with $V_{dd} = 1V$ and capacitive load of $10fF$ at the output nodes ($Dp$ and $Dn$) of all comparators.

*1) Power consumption versus input common mode voltage:* The power consumption of the proposed comparator with respect to the input common mode voltage was simulated and compared with other structures for $1mV$ differential input. The results are shown in Fig. 6. The low power consumption of the proposed and conventional double tail comparators is due to the absence of static power dissipation. Also, the power consumption of the comparator in [4] increased significantly with input common mode voltage. This is because of the hidden static power in the latching phase that was explained in section II.

*2) Delay versus input common mode voltage:* The effect of input common mode voltage on the delay of comparators was simulated for $1mV$ differential input and the results shown in Fig. 7. The delay of the proposed comparator is not sensitive to the input common mode voltage. Double tail comparator is fast for high values of common mode voltages and slow for low values of common mode voltages.

*3) Comparators offset versus input common mode voltage:* The comparators offset variations were simulated for different values of input common mode voltages and the results shown in Fig. 8. It can be seen that the proposed comparator shows

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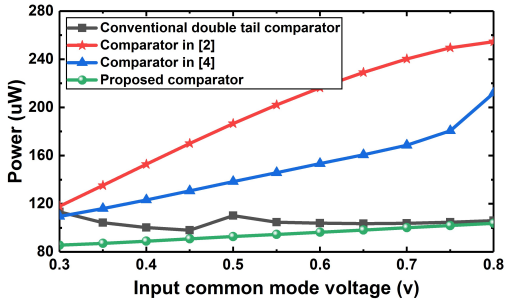


Fig. 6. Power consumption versus input common mode voltage.

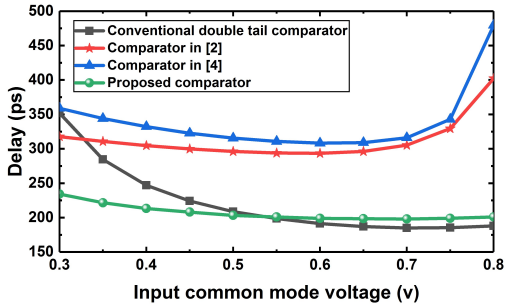


Fig. 7. Delay versus input common mode voltage.

less fluctuation with respect to input common mode variations, which makes it suitable for recent SAR ADCs with energy efficient switching.

Also, the trade-off between speed and offset in conventional double tail comparator is shown in Fig. 7 and Fig. 8. Variation of offset with input common mode voltage has significant impact on the total linearity of SAR ADCs [5] with switching schemes, which have a large variation of the common mode voltage in their differential DAC.

*4) Delay versus input differential voltage:* The simulated delays are illustrated in Fig. 9. For fair comparison, common mode voltage is set to $500mV(0.5V_{dd})$. As it can be seen, the proposed comparator has the highest speed among its counterparts.

*5) Other Simulations:* Fig. 10 illustrates the result of the Monte Carlo simulation of the proposed comparator. As it can be seen, the offset voltage of $\sigma os = 5.22mV$ is achieved.

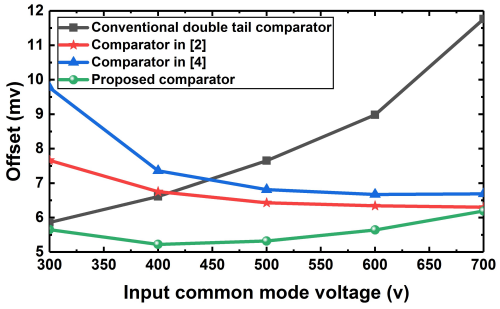


Fig. 8. Comparators offset versus input common mode voltage

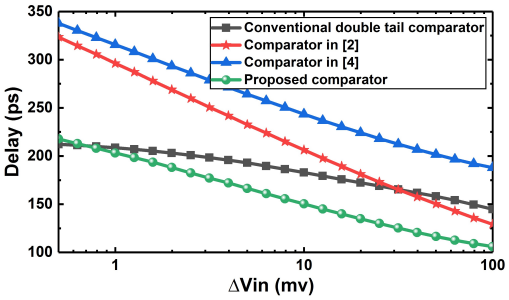


Fig. 9. Delay versus input differential voltage.

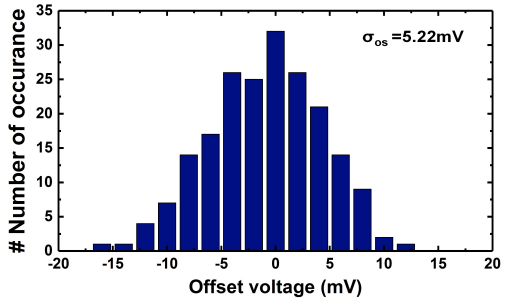


Fig. 10. Distribution of the offset voltage in the proposed comparator from Monte Carlo simulation.

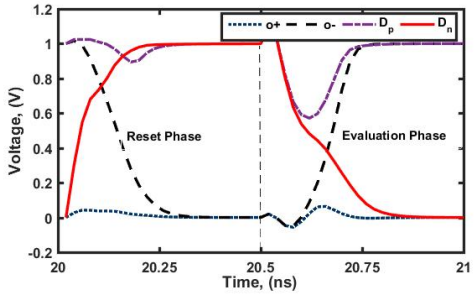


Fig. 11. Transient simulation of the proposed comparator.

Finally, the transient waveforms of the proposed comparator for the $Vcm = 0.4V$ and input frequency of $1GHz$ are shown in Fig. 11.

## V. Conclusion

A new low power and high speed dynamic comparator structure is proposed. The pre-amplifier is directly connected to the latch without significant capacitive load. Static power consumption is avoided through switches that will be controlled by output logics. The simulation results illustrate that the proposed structure shows less delay and power consumption. Also, good offset performance over wide common mode range is achieved.

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