Adjustable Hysteresis CMOS Schmitt Triggers

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***Abstract*— Adjustable hysteresis CMOS Schmitt trigger design strategies are investigated and two new inverter based designs are proposed. The sizing of the two feedback inverters controls the two trip points of the structure independently. By the addition of voltage controlled current sinking and/or sourcing transistors, the hysteresis window can be easily moved without changing its width. Moreover the new designs are immune to the kick-back noise coming from the succeeding blocks.**

***Keywords*—Schmitt Trigger, trip point, hysteresis, inverter**

I. INTRODUCTION

Schmitt triggers are used extensively in digital and analog systems to filter out any noise present on a signal line and produce a clean digital signal. These blocks find their way into many instrumentation and test measurement systems. The demand for implementation of controllable hysteresis Schmitt triggers has increased in such systems. The traditional method of implementing a Schmitt trigger is to use a resistive regenerative (positive) feedback amplifier [1]. The basic idea of a Schmitt trigger is to generate a bi-stable state which has a switching threshold as a function of the direction of the input. The main drawbacks of this implementation are mainly related to op-amp design challenges, e.g. large die area, high DC gain requirements, low offset requirements etc. Another disadvantage of such an implementation is the high power requirement which makes this structure unfavorable in many analog and digital systems. Another approach for implementation is to use standard CMOS inverters along with positive feedback (e.g. latches) [2-4]. The basic idea proposed in [2] is to provide an active alternate pull down path for the output of the first inverter when the input is changing from high to low. The alternate pull down path keeps pulling down the output of the first inverter even beyond the quasi-static (or the trip point) of the inverter. When the input is changing from low to high, this alternate path is actually inactive and thus the trip point will be determined primarily by only the input inverter. This idea can be easily extended to a complementary design where an alternate pull up path is also present [3]. For hysteresis adjustment, the author in [4] introduced an additional voltage controlled transistor in the feedback path. This adjustment is actually non-linear with respect to the controlling voltage.

In all of these designs one key performance determining block has been neglected. This block is the output inverter which is also present in the feedback path. The sizing of the output inverter will also affect in the trip points of the Schmitt trigger. Another drawback of the present implementation schemes is related to the kick-back noise coming from other digital/analog blocks connected to the Schmitt trigger's output. To address this issue, the output inverter can be separated out from feedback inverters. By doing this, the feedback node will be internal to the Schmitt trigger and hence the design will be more immune to the kick-back noise. Additional advantage of such an approach is that the same inverter sizing for both pull-up and pull-down feedback paths is not required. By using different inverter sizing, the trip points of the Schmitt trigger can easily by varied to compensate for power supply, process and temperature variations. One can also introduce hysteresis adjustable design as described in [4] into this new design scheme. A different approach for adjusting the trip points of the Schmitt trigger, without affecting the hysteresis width too much, is to introduce voltage controlled current source/sink at the output of the input inverter at a price of small power consumption.

In section II, the basic operation of a traditional inverter based Schmitt trigger will be discussed which will be followed by new Schmitt trigger designs in section III. Simulation comparison of these structures will be covered in section IV and the conclusions will be summarized in section V.

II. TRADITIONAL INVERTER BASED SCHMITT TRIGGERS

A commonly used Schmitt trigger design is shown in the Fig. 1 [2-3]. This structure has two inverters ($INV_{I/P}$ and $INV_{O/P}$) and two feedback transistors ($NMOS_{FB}$ and $PMOS_{FB}$). For analyzing this structure, first assume that no feedback transistors are present. This case will be just a cascading of two inverters and the O/P transition point (or quasi-static point, V_{QS}) will be primary defined by the $INV_{I/P}$ dimensions. Now assume that V_{IN} is high, V_{INT} is low and V_{OUT} is high and the $NMOS_{FB}$ transistor is also present. The gate of $NMOS_{FB}$ transistor is connected to the V_{OUT}, which is high, hence this transistor will be pulling the V_{INT} node to the low voltage also. This is basically generating a positive feedback in the system. If V_{IN} decreases from high to low, $NMOS_{FB}$ transistor will keep on pulling the V_{INT} node to the low voltage even after the input crosses the V_{QS} point. The $NMOS_{FB}$ transistor turns off only when the V_{INT} goes above the quasi-static point of the output inverter causing V_{OUT} to go low and at that time the system starts to work as normal cascaded inverters. The transition or the trip point occurs when the pole of the system crosses $j\omega$ axis. At that transition point, the input inverter's transistors are in saturation, the output inverter's NMOS and PMOS are in saturation and triode, respectively, and the feedback NMOS

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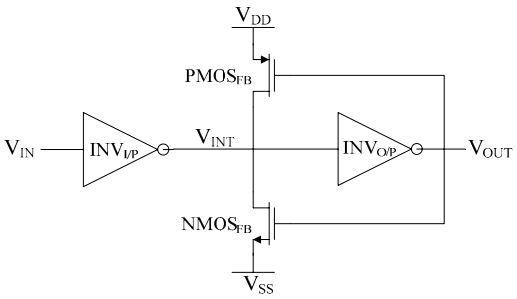

Figure 1. Traditional inverter based Schmitt Trigger (Str. 1)

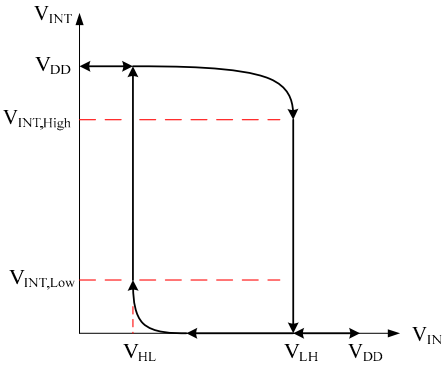

Figure 2. Hysteresis curve for V_{INT} vs V_{IN}

transistor is in triode region. One can formulate a set of three non-linear equations for finding the High to Low trip point (V_{HL}), V_{INT} and V_{OUT}. Out of these three equations, one will reflect the pole movement across $j\omega$ axis and the other two would be KCL at the V_{INT} and V_{OUT} nodes. Similarly, if the $PMOS_{FB}$ transistor is present in the system, it would introduce another positive feedback and will affect the Low to High trip point (V_{LH}) of the system. Fig. 2 shows a typical hysteresis for V_{INT} vs. V_{IN}. The $V_{INT,High}$ and $V_{INT,Low}$ voltages are the V_{INT} node voltages at V_{LH} and V_{HL}, respectively. The adjustment of the trip points is possible by varying the sizing of the input inverter transistors along with the sizing of the feedback transistors [2-4]. Another possible trip point adjustment is by changing the output inverter dimensions. This effect has been neglected in the literature for such kind of positive feedback Schmitt triggers. One issue with these structures is related to the kick-back noise coming from the circuitry connected to the output node of the Schmitt trigger. The output node is connected to the feedback transistors and can easily affect the performance of the overall structure in presence of the kick-back noise.

Based on the observations that the output inverter sizing plays a role in determining the trip points along with the kick-back noise problem, two new structures have been investigated in the next section.

III. New Schmitt Trigger Design

A new Schmitt trigger design is shown in the Fig. 3. The first step in the new design is splitting the output inverter of

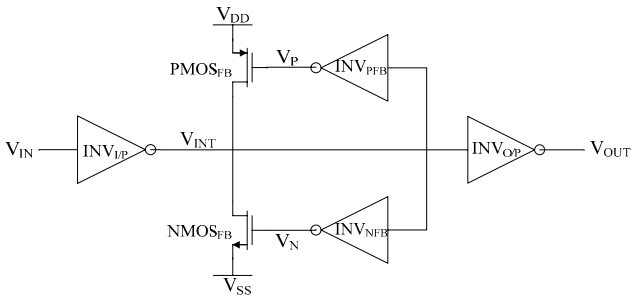

Figure 3. Proposed Schmitt Trigger design (Str. 2)

Fig. 1 into three inverters ($INV_{O/P}$, INV_{PFB} and INV_{NFB}) as shown in the Fig. 3. If all three inverters have same transistor dimensions as in traditional case, then the trip points will be exactly the same as before. The splitting of the output inverter has two advantages over the previous structure. The first positive point of the new structure is freedom of independent transistor sizing of the two feedback inverters. This independent inverter sizing will result in nearly independent control of the two trip points. The second positive point is reduction in the kick-back noise as the output node is not in the feedback path. But this new structure has a new design challenge for the output inverter ($INV_{O/P}$). The design constraint will come from the $V_{INT,High}$ and $V_{INT,Low}$. These values will change when the feedback inverters' dimensions are changed. To ensure the proper operation of this new Schmitt trigger, the quasi-static point (or the trip point) of the inverter should be bounded by the maximum of the $V_{INT,Low}$ and the minimum of the $V_{INT,High}$. For a design where this is a challenge, the output can be tapped from V_P or V_N followed by 2 cascaded inverters at an expense of longer propagation delay. But still there is flexibility of adjusting the trip points independently. Another modification to this new Schmitt trigger design is to include the V_{OUT} in the feedback path in such a way that it doesn't introduce a direct path for kick-back noise. One such method is shown in Fig. 4 where the feedback inverters are modified to include two inputs (V_{INT} and V_{OUT}) rather than one. These modified inverters (INV_{2NFB} and INV_{2PFB}) are shown in Fig 5 and Fig. 6. These two input inverters have same functional implementation as that of a single input inverter. With this implementation scheme, the V_{OUT} is in the positive feedback loop and hence the $V_{INT,High}$ and $V_{INT,Low}$ will track the sizing of the output inverter. Therefore, the output inverter sizing will not hamper the performance of the overall Schmitt trigger.

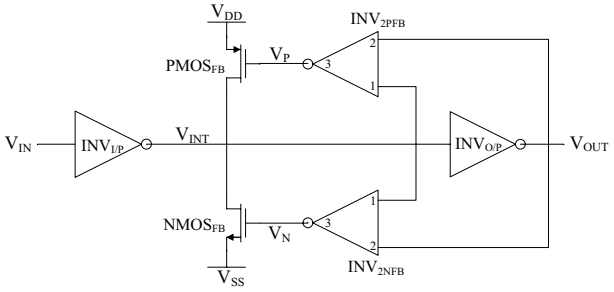

Figure 4. Modified Proposed Schmitt Trigger design (Str. 3)

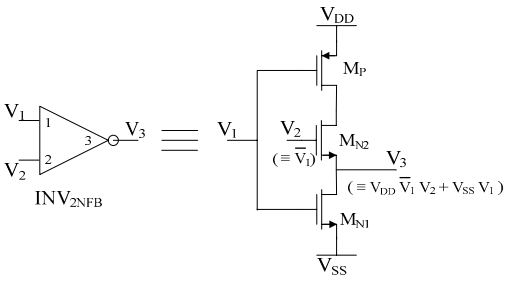

Figure 5. Two input inverter for $NMOS_{FB}$ (INV_{2NFB})

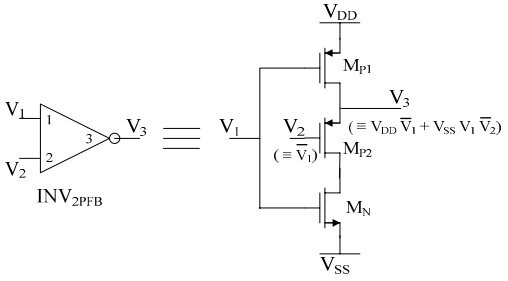

Figure 6. Two input inverter for $PMOS_{FB}$ (INV_{2PFB})

Another possible modification to these structures is addition of voltage controlled current sinking and/or sourcing transistors at V_{INT} node. The addition of such transistors will shift the hysteresis window without changing the width of the hysteresis much. Yet another modification to these new designs would involve the trip point control as shown in [4]. Use of these techniques can help in better control of the adjustment of the trip points.

IV. Simulation Results

The traditional design, Fig. 1 (Str. 1), and the two proposed designs, Fig. 3 (Str. 2) and Fig. 4 (Str. 3), are designed in TSMC 0.18µm process. Key values used for these structures are listed in Table I. For generating the hysteresis curve, a triangular input from rail to rail power supply with a frequency of 50Hz is used. For comparison between these structures, all transistor widths of the feedback inverters are sized 1µm. Different $NMOS_{FB}$ and $PMOS_{FB}$ sizes are used to achieve similar trip points in all the three cases. For the traditional design (Str. 1), the output inverter sizing of 1µm will not be used in an application as this inverter is also the output driving inverter. But for studying the effects of the feedback inverter sizing on the trip points, the nominal sizing of 1µm will be reasonable. For these transistors sizing scheme, the high to low trip point (V_{HL}) is approximately 0.49V (i.e. 24.5% w.r.t. V_{DD}) and the low to high trip point (V_{LH}) is approximately 1.57V (i.e. 78.5% w.r.t. V_{DD}). Each feedback inverter's transistor size is varied from 1µm to 20µm one at a time while keeping the others unchanged and V_{HL}, V_{LH}, $V_{INT,Low}$ and $V_{INT,High}$ are noted down for all 3 designs. Tables II-VI summarizes these data. The information stored in the trip points can be viewed by looking at the change in the hysteresis width and its mid-point value. From the traditional design's (Str. 1) data (Table II), the

TABLE I. Key values used for simulations

Power Supply	V_{DD} = 2V, V_{SS} = 0V
Length (L) for all transistors	0.4µm
$INV_{I/P}$ (for all structures)	Width of NMOS: 2µm
	Width of PMOS: 8.3µm
$INV_{O/P}$ (for Str. 2 and 3 only)	Width of NMOS: 4µm
	Width of PMOS: 17µm
Feedback Inverters (for Str. 2 and the $INV_{O/P}$ of Str. 1)	Width of NMOS: 1µm
	Width of PMOS: 1µm
INV_{2NFB} of Str. 3 (feedback inverter)	Width of M_{N1}: 1µm
	Width of M_{N2}: 1µm
	Width of M_P: 1µm
INV_{2PFB} of Str. 3 (feedback inverter)	Width of M_N: 1µm
	Width of M_{P1}: 1µm
	Width of M_{P2}: 1µm
Str. 1 and 2 Feedback transistors	Width of $NMOS_{FB}$: 1.8µm
	Width of $PMOS_{FB}$: 5µm
Str. 3 Feedback transistors	Width of $NMOS_{FB}$: 3.7µm
	Width of $PMOS_{FB}$: 16.6µm
Simulation Temperature	50°C

hysteresis width changes only by around 8.8% w.r.t. V_{DD} and the hysteresis mid-point changes by 19.5% w.r.t. V_{DD} implying that by changing the output inverter sizing both V_{HL} and V_{LH} track each other reasonably. This was actually expected as both the feedback paths use same inverter. For the proposed design (Str. 2), when only INV_{NFB} is varied (Table III), the hysteresis width changes by 9.6% w.r.t. V_{DD} and the mid-point change is 5.6%, hence the INV_{NFB} is affecting the V_{HL} trip point primarily and has little influence on the V_{LH} trip point. Structure 2 with INV_{PFB} varying (Table IV), the hysteresis width and mid-point values changes by 13.3% and 7.2% w.r.t. V_{DD}, respectively, which implies INV_{PFB} primarily influences V_{LH} rather than V_{HL}. For this proposed structure one design challenge was noted for the output inverter sizing in the previous section. This point is evident from the data of $V_{INT,Low}$ and $V_{INT,High}$ in Tables III and IV. The maximum value of $V_{INT,Low}$ is around 37% and the minimum value of $V_{INT,High}$ is around 39% leaving a margin of only 2% to set the quasi-static point (or the trip point) of the output inverter in that range. This will be hard to achieve with the process and temperature variations. The adjustable range of the trip points have to be sacrificed for a better head room for the design of the output inverter. When we go to the modified proposed design (Str. 3), this worst difference between $V_{INT,Low}$ and $V_{INT,High}$ is around 50% (i.e. 1V) as shown by the data in Tables V and VI. This large head room is achieved by introducing the output into the feedback paths without adding any kick-back noise into the system. For Str. 3 with INV_{2NFB} varying (Table V), the hysteresis width and mid-point values change by 10.6% and 5.3% and for the case where INV_{2PFB} is varied (Table VI) these values are 15.2% and 7.6%, respectively. In the modified proposed structure, the simulation data also shows independent control of the trip points by varying the respective inverter size alone. Therefore, total hysteresis width change of 25% is achievable along with 12.5% change in the mid-point of the hysteresis. Typically these large controllable ranges will be sufficient to compensate for any process or temperature variations. Simulations also show that the output inverter sizing has little impact on the trip points of the design of the Str. 3.

The main advantage of adding V_{OUT} into the feedback path by utilizing 2 input inverter scheme is the increase in the separation of the $V_{INT,Low}$ and $V_{INT,High}$.

Other important performance characterization factors of a Schmitt trigger's trip points are with respect to temperature and power supply. For these two cases all the transistors' widths are kept constant to the values given in Table I and only temperature or the power supply was changed. Simulation data for these two cases are shown in Tables VII and VIII. For these set of simulations both traditional design (Str. 1) and proposed design (Str. 2) have identical sizing, hence they have the same results. For the temperature variation and the power supply variation cases, all structures performed in a similar manner with only small performance improvement of the Str. 3 over the other two.

The two additional modifications mentioned in the previous section, addition of voltage controlled current sinking and/or sourcing transistor(s) at V_{INT} node and the scheme mentioned in [4], will also enhance the performance of the two proposed structures without adding much to the die area.

V. CONCLUSIONS

Two new Schmitt trigger designs were presented. As opposed to the traditional implementation scheme, the new design approach used two separate inverters for each positive feedback paths. This modification resulted in near independent trip point control by varying the sizing of the respective feedback inverter in the first proposed design. In the second proposed design, the feedback inverters were modified to include two inputs, one from the internal node of the Schmitt trigger and the other being the output node, which resulted in independent control of the trip points by the sizing of the respective two input inverters. Simulations for these structures showed wide trip point control by varying feedback inverters sizing, specifically by the latter modification utilizing two input inverter scheme. The proposed structures also have added advantage of reduced kick back noise. These structures can also have current sourcing and/or sinking voltage controlled transistors at the output of the input inverter, which can shift the hysteresis window without changing its width. Splitting of the inverters for separate feedback paths along with the use of two input inverters are not limited to the present architecture, but can be used in other Schmitt trigger designs making them more favorable to different applications.

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TABLE II. TRIP POINT VARIATION VS. FEEDBACK INVERTER FOR STR. 1

INV_{OUT} (W_N, W_P) (μm)	(% w.r.t. V_{DD})			
	V_{HL}	V_{LH}	$V_{INT,Low}$	$V_{INT,High}$
(1, 1)	24.46	78.31	31.28	48.52
(1, 5)	19.70	72.91	40.96	60.90
(1, 20)	15.40	69.02	54.10	68.43
(5, 1)	28.16	84.33	25.03	33.38
(20, 1)	30.71	92.71	21.86	27.04

TABLE III. TRIP POINT VARIATION VS. INV_{NFB} FOR STR. 2

INV_{NFB} (W_N, W_P) (μm)	(% w.r.t. V_{DD})			
	V_{HL}	V_{LH}	$V_{INT,Low}$	$V_{INT,High}$
(1, 1)	24.46	78.31	31.28	48.52
(1, 5)	20.32	77.54	37.24	52.89
(5, 1)	28.16	78.31	25.04	48.47
(20, 1)	30.71	78.31	21.79	48.27

TABLE IV. TRIP POINT VARIATION VS. INV_{PFB} FOR STR. 2

INV_{PFB} (W_N, W_P) (μm)	(% w.r.t. V_{DD})			
	V_{HL}	V_{LH}	$V_{INT,Low}$	$V_{INT,High}$
(1, 1)	24.46	78.31	31.28	48.52
(1, 5)	24.46	72.91	31.26	60.90
(1, 20)	24.46	69.02	30.88	68.53
(5, 1)	25.01	82.86	29.31	39.31

TABLE V. TRIP POINT VARIATION VS. INV_{2NFB} FOR STR. 3

INV_{2NFB} (W_{N1}, W_{N2}, W_P) (μm)	(% w.r.t. V_{DD})			
	V_{HL}	V_{LH}	$V_{INT,Low}$	$V_{INT,High}$
(1, 1, 1)	24.80	78.30	20.87	78.70
(1, 5, 1)	21.76	78.30	23.94	78.90
(1, 20, 1)	19.41	78.30	24.50	79.19
(5, 1, 1)	27.71	78.30	18.93	78.90
(20, 1, 1)	30.05	78.30	17.02	78.90

TABLE VI. TRIP POINT VARIATION VS. INV_{2PFB} FOR STR. 3

INV_{2PFB} (W_N, W_{P1}, W_{P2}) (μm)	(% w.r.t. V_{DD})			
	V_{HL}	V_{LH}	$V_{INT,Low}$	$V_{INT,High}$
(1, 1, 1)	24.80	78.30	20.87	78.70
(1, 5, 1)	24.80	74.26	21.04	81.53
(1, 20, 1)	24.80	71.19	20.91	83.42
(1, 1, 5)	24.80	82.72	21.05	76.76
(1, 1, 20)	24.80	86.44	21.64	74.46

TABLE VII. HYSTERESIS VARIATION VS. TEMERATURE

Temp. (°C)	(% w.r.t. V_{DD})			
	Str. 1 and Str. 2		Str. 3	
	Hyst. Width	*Hyst. Mid-pt.*	*Hyst. Width*	*Hyst. Mid-pt.*
-50	58.89	45.18	58.76	45.79
0	56.02	48.26	54.92	48.32
50	53.84	51.38	53.49	51.55
100	52.62	54.27	53.07	54.57
150	52.16	56.97	53.26	57.40

TABLE VIII. HYSTERESIS VARIATION VS. POWER SUPPLY

V_{DD} (V)	(% w.r.t. V_{DD})			
	Str. 1 and Str. 2		Str. 3	
	Hyst. Width	*Hyst. Mid-pt.*	*Hyst. Width*	*Hyst. Mid-pt.*
1.5	63.54	47.50	48.42	49.24
2	53.84	51.38	53.49	51.55
2.5	49.80	54.34	59.62	54.73