Low-voltage high-speed Schmitt trigger and compact window comparator

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Gates with input hysteresis are often necessary in circuits operating in noisy environments. Described is a very simple CMOS Schmitt trigger circuit, well suited for low-voltage and high-speed applications. The circuit also allows the construction of a very compact window comparator.

Introduction: Gates with voltage hysteresis are frequently needed in systems operating with noisy inputs. Two well-known Schmitt trigger (ST) implementations are shown Figs. 1*a* and *b*. Owing to its four-transistor pile-up, the structure of Fig. 1*a* [1] is not as well suited for low-voltage (LV) applications as that of Fig. 1*b* [2]. However, in the latter, because of the contention between the strong inverter (M1-M2) and the weak inverter (M3-M4) on node X (which constitutes the basic operating principle of that ST), its speed is reduced. A new approach is presented in Fig. 1*c*, along with its typical DC response (Fig. 1*d*). This circuit is also suitable for LV applications; however, the speed reduction problem is solved by letting the circuit go into a 'floating' state before any transition occurs.

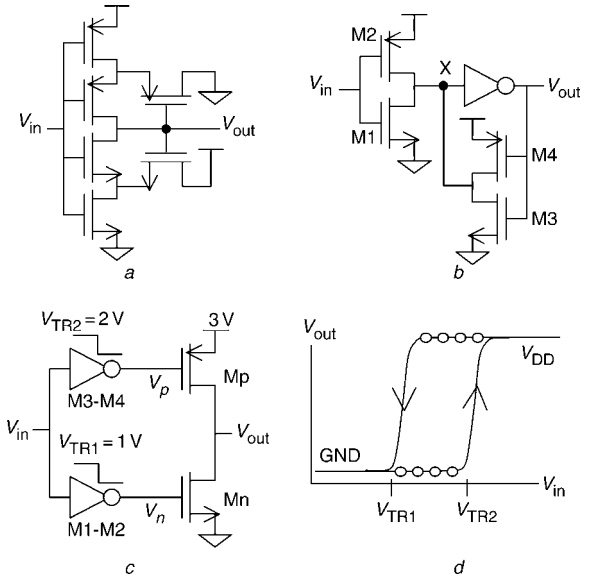

Fig. 1 *Schmitt trigger circuits*

a, *b* Traditional implementations
c Proposed circuit
d Typical response (little circles indicate 'floating' state)

Circuit description: The proposed ST circuit (Fig. 1*c*) is composed of two regular CMOS inverters (M1-M2 and M3-M4), plus two output transistors (Mn-Mp). When $V_{in} = 0$ V, $V_n = V_p = 3$ V (with $V_{DD} = 3$ V), so only Mn is on, $V_{out} = 0$ V. Similarly, when $V_{in} = 3$ V, $V_n = V_p = 0$ V, thus only Mp is on and $V_{out} = 3$ V. Notice, however, that each inverter has a distinct transition voltage ($V_{TR1} = 1$ V for the lower inverter, $V_{TR2} = 2$ V for the upper one). Therefore, as V_{in} goes from 0 to 3 V, it first deactivates Mn, thus causing both output transistors (Mn-Mp) to be off momentarily (for $1\text{ V} < V_{in} < 2\text{ V}$). This situation is depicted by the little circles in Fig. 1*d*. Consequently, when V_{in} reaches 2 V, Mp is turned on, with no contention between Mn and Mp occurring (because Mn was already off). The result is a much faster transition. A similar analysis can be made for V_{in} returning from 3 to 0 V. The amount of hysteresis is given by $V_{TR2} - V_{TR1}$.

The determination of V_{TR} for each CMOS inverter is straightforward. Calling the inverter's *n*-type transistor by Mn_{inv} and the *p*-type by Mp_{inv}, and equating their drain currents when both go through the saturation region, results in $V_{TR} = [k(V_{DD} - V_{Tp}) + V_{Tn}]/(k+1)$, where $k = (\beta_n/\beta_p)^{1/2}$, β_n and β_p are the transconductance factors of Mn_{inv} and Mp_{inv}, respectively (with $\beta = \mu C_{OX} W/L$), and V_{Tn} and V_{Tp} are their respective threshold voltages. Therefore, by designing k (i.e. W/L) properly, the desired transition voltages V_{TR1} and V_{TR2} are obtained. A few examples, for $V_{DD} = 3.3$ V, $V_{Tn} = 0.65$ V, and $V_{Tp} = -0.95$ V, are shown in Table 1.

Table 1: Examples of V_{TR} values

V_{DD}	V_{Tn}	V_{Tp}	k	V_{TR} (V)
3.3 V	0.65 V	−0.95 V	0.5	1.22
			1	1.50
			2	1.78
			4	2.01

Window comparator: The principle can also be extended to attain a very compact window comparator. A conventional window comparator is shown in Fig. 2*a*, which consists of two voltage comparators connected to an AND gate, producing $V_{out} =$ '1' when $V_L < V_{in} < V_H$, or $V_{out} =$ '0' otherwise. The new circuit is shown in Fig. 2*b*. Instead of voltage comparators (which are large circuits), it employs just three simple two-transistor inverters, the operation of which is again based on distinct transition voltages. With $V_{DD} = 3$ V, $V_{TR1} = 2$ V, and $V_{TR2} = 1$ V, for example, $V_{out} = 3$ V when $1\text{ V} < V_{in} < 2$ V, or $V_{out} = 0$ V otherwise. This approach is suitable for LV, high-speed implementations that do not require V_H and V_L to be highly accurate and programmable.

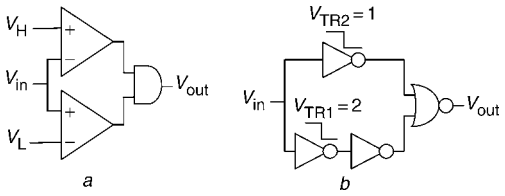

Fig. 2 *Window comparators*

a Conventional
b Proposed

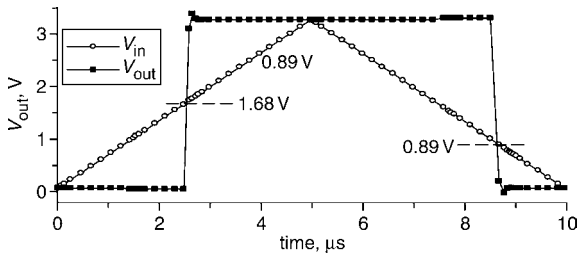

Fig. 3 *Hysteresis measurements*

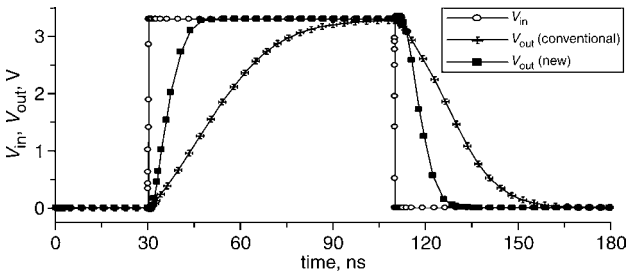

Fig. 4 *Speed comparison between conventional ST (Fig. 1b) and proposed circuit (Fig. 1c)*

Results: Simulation results, with AMI 0.5 µm CMOS parameters, are reported next. Fig. 3 shows hysteresis measurements regarding the proposed ST (Fig. 1*c*), with the following transistor sizes (in units of lambda): $(W/L)_{1,p} = 6/2$, $(W/L)_{2,3,n} = 3/2$, and $(W/L)_4 = 12/2$. $V_{DD} = 3.3$ V was employed in all tests. The observed transition voltages were $V_{TR1} = 0.89$ V and $V_{TR2} = 1.68$ V, resulting in 0.79 V of hysteresis. A speed comparison between the proposed ST and that of Fig. 1*b*, designed with comparable transistor sizes and with the same capacitive load (1pF), is presented in Fig. 4, where the predicted superiority of the new circuit is apparent. Finally, Fig. 5 shows simulation results regarding the DC response of the proposed

window comparator (Fig. 2*b*), with the results again confirming the predicted behaviour.

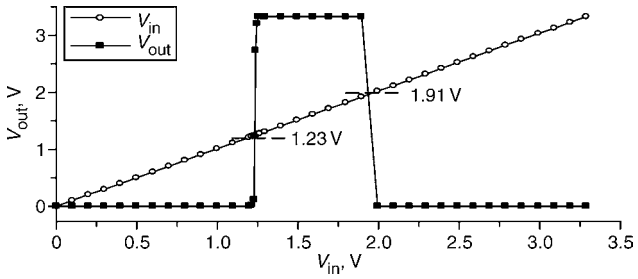

Fig. 5 *Simulation results of window comparator*

Conclusions: A new technique for the design of ST circuits has been presented and tested, which allows LV operation, with higher speed than traditional approaches. The principle was then extended to the construction of a very compact window comparator (only eight transistors), suitable for applications where neither high accuracy nor programmability of the high/low window voltages are required.

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