Low voltage CMOS Schmitt trigger circuits

C. Zhang, A. Srivastava and P.K. Ajmera

Two new low voltage Schmitt trigger circuits are presented which use dynamic body-bias technique. The first circuit is designed for operation at 1 V. The second circuit, derived from the first circuit, is designed for operation at 0.4 V. Experimental results for the new Schmitt trigger circuits are presented.

Introduction: Schmitt trigger circuits are widely used for waveform shaping under noisy conditions in electronic circuits [1, 2]. In VLSI circuits, they are often used at the chip input side and as single-ended receivers in DRAMs [3, 4]. The hysteresis in a Schmitt trigger offers better noise margin and noise stable operation. With proliferation of portable devices, low power circuits are extremely desirable. In a recent work [5], a low power Schmitt trigger circuit design is reported for 3 V operation. The cascade architecture used in this design limits lowering the operating voltage. In this Letter, we report novel Schmitt trigger circuit designs in CMOS for operation at 1 V and below using a dynamic body-bias method [6].

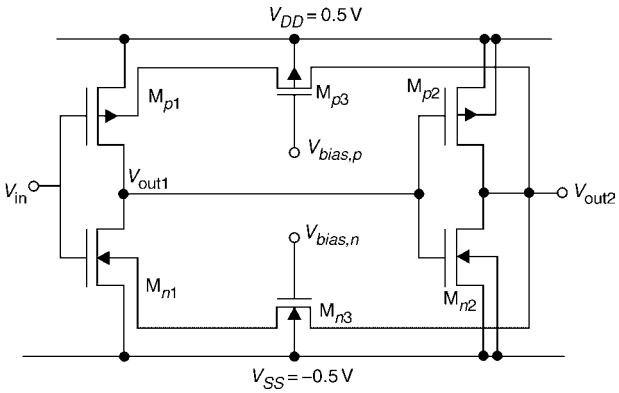


Fig. 1 *1 V CMOS Schmitt trigger circuit*

CMOS Schmitt trigger circuit design and prototyping: Fig. 1 shows the proposed 1 V Schmitt trigger circuit. In this design, a dynamic body-bias is applied to a simple CMOS inverter circuit, whereby the threshold voltages of the two MOSFETs can be changed, thus changing the switching voltage. The operation of the circuit of Fig. 1 can be described as follows. First, the values of bias voltages $V_{bias,p}$ and $V_{bias,n}$ are, respectively, set externally to values $(-|V_{thp3}|+0.1)$ V and $(V_{thn3}-0.1)$ V. This ensures that the drain voltage magnitudes of the MOSFETs M_{p3} and M_{n3} (body voltage magnitudes of the MOSFETs M_{p1} and M_{n1}) will have a value of +0.1 V minimum, and −0.1 V maximum, respectively, when the transistor is conducting. This will limit forward body-bias in transistors M_{n1} and M_{p1} to 0.4 V. A forward bias greater than 0.4 V may trigger latch-up in a CMOS circuit [7]. When a low value signal is applied to V_{in}, V_{out2} goes low. V_{out2} provides zero forward body-bias to the transistors of M_{n1} through M_{n3} operating in linear region and a forward bias of 0.4 V to M_{p1} through M_{p3} operating in saturation region. The substrate of transistor M_{n1} is biased at −0.5 V and its threshold voltage now corresponds to the value at zero substrate bias, $V_{tho,n1}$, while the substrate of transistor M_{p1} is biased at +0.1 V with its threshold voltage corresponding to +0.4 V forward-bias value, $V_{th,p1}$.

Transistor M_{p1} remains on and M_{n1} remains off until V_{in} increases to a certain voltage V_{hl}, at which output, V_{out1} switches from a high to a low value and V_{out2} switches from a low to a high value. Since M_{n1} substrate is zero body-bias, its threshold voltage $V_{tho,n1}$ is higher than the value for forward body-bias. Hence, a higher voltage is needed to turn M_{n1} on. For a ramp input, this results in a time delay t_1, as V_{out1} goes to a low value and V_{out2} goes to a high value of V_{DD}. This provides a 0.4 V forward body bias to M_{n1} through the transistor M_{n3} operating in saturation at the end of the switching transient period. A zero body-bias is now provided to M_{p1} through the transistor M_{p3} operating in the linear region at the end of the switching transient. Transistor M_{p1} is now off and M_{n1} remains on until V_{in} decreases to a certain voltage V_{lh}, at which output, V_{out1} switches from low to high and V_{out2} switches from high to low. Since M_{n1} has forward substrate body-bias, a lower voltage is now needed to turn it off. This results in a time delay t_2 for a ramp input. The different switching voltage or switching time causes the hysteresis. V_{out1} is buffered by an M_{p2}–M_{n2} inverter, which provides high fan-out capability. Thus, output is taken at the V_{out2} terminal.

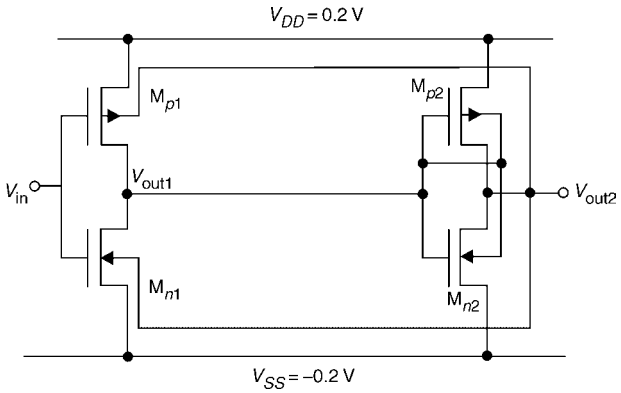
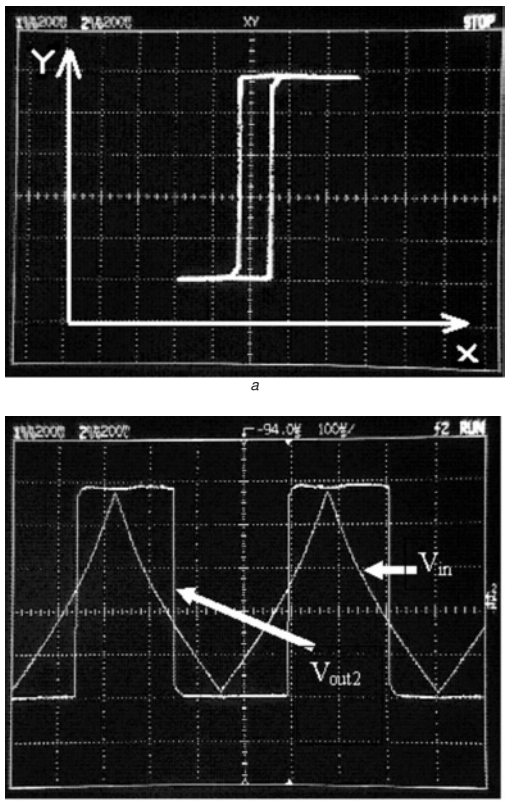


Fig. 2 *0.4 V CMOS Schmitt trigger circuit derived from Fig. 1*



a

b

Fig. 3 *Measured hysterisis characteristics of 1 V CMOS Schmitt trigger circuit (Fig. 1), and measured input–output waveform characteristics*

a Measured hysterisis characteristics (V_{out2} against V_{in}) of 1 V CMOS Schmitt trigger circuit in Fig. 1
b Measured input–output (V_{in}–V_{out2}) waveform characteristics
x-axis = 0.2 V/div., y-axis = 0.2 V/div., V_{in} = −0.5 to +0.5 V

The switching voltage V_{hl} can be calculated using the following equations:

$$\frac{\beta_n}{2}(V_{hl}-V_{tho,n})^2=\frac{\beta_p}{2}(V_{DD}-V_{hl}-|V_{th,p}|)^2 \quad (1)$$

and,

$$V_{hl}=\frac{V_{DD}-|V_{th,p}|+R\times V_{tho,n}}{R+1} \quad (2)$$

where, $\sqrt{(\beta_n/\beta_p)}=R$, β_n and β_p are transconductance parameters of n- and p-MOSFETs, respectively. $V_{tho,n}$ is the zero substrate body-bias

threshold voltage of the n-MOSFET, $V_{th,p}$ is forward substrate body-bias threshold voltage of the p-MOSFET, V_{DD} is the supply voltage.

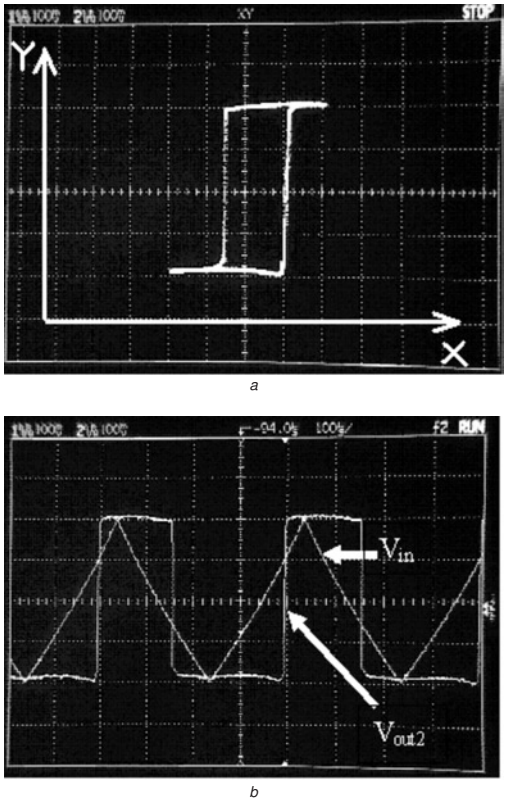
A similar analysis can be used to calculate V_{lh}:

$$V_{lh} = \frac{V_{DD} + R \times V_{th,n} - |V_{tho,p}|}{R+1} \quad (3)$$

where, $V_{th,n}$ is the forward substrate body-bias threshold voltage of the n-MOSFET, $|V_{tho,p}|$ is the zero substrate body bias threshold voltage of the p-MOSFET. Hysteresis width V_{hw} is calculated as follows:

$$V_{hw} = V_{hl} - V_{lh} = \frac{(|V_{tho,p}| - |V_{th,p}|) + R \times (V_{tho,n} - V_{th,n})}{R+1} \quad (4)$$

Fig. 2 shows a CMOS Schmitt trigger circuit design for operation at an extreme low voltage value of 0.4 V. The configuration of Fig. 2 does not allow the forward body-bias to exceed 0.4 V. Thus, the transistors M_{p3} and M_{n3} shown in the circuit of Fig. 1 are not required in the circuit of Fig. 2. The configuration of M_{p2} and M_{n2} is called dynamic threshold MOS (DTMOS) [6] inverter that ensures the inverter operation at ultra-low voltage of 0.4 V.



a

b

Fig. 4 *Measured hysterisis characteristics of 0.4 V CMOS Schmitt trigger circuit (Fig. 2), and measured input–output waveform characteristics*

a Measured hysterisis characteristic of 0.4 V CMOS Schmitt trigger circuit in Fig. 2

b Measured input–output (V_{in}–V_{out2}) waveform characteristics

x-axis = 0.1 V/div., y-axis = 0.1 V/div., V_{in} = −0.2 to +0.2 V

Figs. 3*a* and *b* show the measured hysterisis and input–output characteristics of a CMOS Schmitt trigger implemented in standard 1.5 µm CMOS process corresponding to the circuit of Fig. 1. Figs. 4*a* and *b* show similar characteristics for the circuit of Fig. 2. The measured hysterisis width, V_{hw}, is close 0.15 V and agrees with the corresponding calculated value of 0.15 V from (4), for 0.4 V forward body-bias and $R = 1$.

Conclusion: CMOS Schmitt trigger circuits have been implemented in standard 1.5 µm CMOS process for operation at 1 and 0.4 V using the dynamic threshold technique. This method exploits lowering of the threshold voltage of a MOSFET under forward substrate body-bias. Measured hysterisis widths agree closely with the corresponding calculated value of 0.15 V. The proposed CMOS Schmitt trigger circuit is extremely useful in low-ultra-low voltage circuit applications.

Acknowledgment: The authors acknowledge partial support of this work through NSF EPSCoR grant 0092001.

2 October 2003
Electronics Letters Online No: 20031131
DOI: 10.1049/el:20031131

C. Zhang, A. Srivastava and P.K. Ajmera (*Electronic Materials and Device Laboratory, Integrated Microsystems Group, Department of Electrical and Computer Engineering, Louisiana State University, Baton Rouge, LA 70803, USA*)

References

1 MILLMAN, J., and GRABEL, A.: 'Microelectronics' (McGraw-Hill, 1987), pp. 679–683
2 SRIVASTAVA, A.: 'Performance characteristics of CMOS Schmitt trigger at liquid nitrogen temperature', *Cryogenics*, 1992, **32**, (7), pp. 671–674
3 GLASSER, L.A., and DOBBERPUHL, D.W.: 'The design and analysis of VLSI circuits' (Addison-Wesley, 1985), pp. 281–283
4 WANG, N.: 'Digital MOS integrated circuits' (Prentice Hall, 1989), pp. 149–155
5 AL-SARAWI, S.F.: 'Low power Schmitt trigger circuit', *Electron. Lett.*, 2002, **38**, (18), pp. 1009–1010
6 ASSADERAGHI, F., *et al.*: 'A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation', *IEDM Tech. Dig.*, 1994, p. 809
7 SRIVASTAVA, A., and GOVINDARAJAN, D.: 'A fast ALU design in CMOS for low voltage operation', *J. VLSI Design*, 2002, **14**, (4), pp. 315–327