New Transformerless STATCOM Topology for Compensating Unbalanced Medium-Voltage Loads

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Abstract

Cascaded multi-level converters have some noticeable advantages such as high reliability, efficient fault management capability, simple structure, and adaptability with different power levels. Furthermore, these converters could be connected to medium-voltage networks without an isolating transformer. However, the voltage balancing of the DC capacitors is a highly challenging task particularly in harmonically polluted and unbalanced systems. To overcome this problem, a new cascaded converter based on two level half-bridge modules for shunt compensators is proposed in this paper. The control algorithm of the compensator and its configuration are designed and optimized in order to achieve an efficient performance in unbalanced systems. This makes it possible to compensate the currents produced by the electric traction system as a popular of medium voltage unbalanced load properly.

Introduction

Modern medium-voltage distribution systems are proliferated with non-linear loads such as single-phase AC traction systems. In addition to the harmonic penetration, these loads enforce significant unbalances to the network. Therefore, the associated problems of reactive and harmonic compensation plus load balancing are inevitable and ought to be considered simultaneously to achieve acceptable power quality level. Meanwhile, mitigation of all these power quality problems by means of a single compensator is a challenging task [1-2]. Previously, static synchronous compensators (STATCOMs) based on multi-pulse voltage source converters were proposed in [3-4], which comprise VSCs and one or more transformers with sophisticated winding connections. These transformers are used to increase the level of output voltage through complex magnetic circuit configurations. On the other hand, such circuit structures produce serious problems like high losses, saturation, non-linear operation of the core plus the effects on the control loop by the compensator, voltage impulse production, high costs and finally, the size.
Cascaded multilevel converter could be directly connected to medium voltage networks [5-6]. Unlike diode-clamped and capacitor-clamped converters, cascaded converters introduce smaller total losses along with higher reliability. But the cascaded converters do have their short comings when operating under distorted unbalance situations in a medium-voltage network compared to those of diode-clamped and capacitor-clamped converters [1-7]. In order to thrash out these limitations, a new STATCOM based on half-bridge cascaded converters (HBCC is proposed in this paper), as shown in Fig. 1(A), which can be used for compensation of reactive power, harmonics and load balancing. The active power exchange in the internal loops of this topology could be used for load balancing, while the voltages of DC capacitors remain balanced. The converter structure and operation is described in Section II. Section III describes control of a basic version of the proposed STATCOM. It is shown that

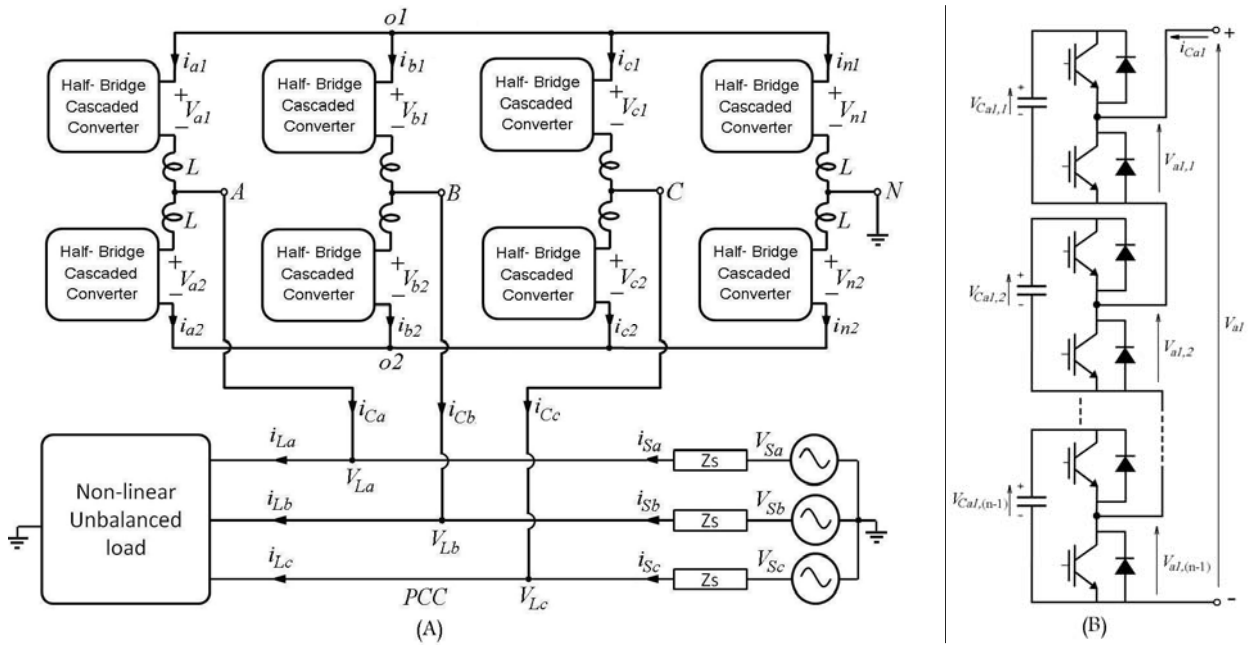

Fig. 1: (A) Configuration of the new transformerless STATCOM topology, (B) Configuration of the upper half-bridge cascaded converter (HBCC) of the proposed converter in phase *a*

the capacitor voltages of the half-bridge modules can be stabilized by proper controlling. Simulations confirm the operation of the basic form of new HBCC based STATCOM.

Converter Description and Operation

The proposed converter of this compensator consists of eight identical HBCC in series with a coupling inductor, in a four-wire system. As shown in figure 1.B, in an *n* level proposed converter, each HBCC is composed of *n-1* identical half-bridge (HB) inverters connected in series. All HB inverters have the same semiconductor-ratings as well as the same capacitance. Therefore, all HB inverters are identical 2-terminal devices .Voltage regulation of the DC-storage capacitors is achieved without any additional connections or energy transfer circuits to the associated HB inverters. Each HB inverter is capable of producing the instantaneous voltages $+V_{Cm}$ and 0 depend on its command signal. Thereupon, according to figure 1(B), terminal voltage of an HBCC can take the value:

$$V_{xm} = V_{xm,1} + V_{xm,2} + \ \dots \ + V_{xm,(n-1)} \quad (1)$$

($x = a, b, c$ or n; and $m = 1$ or 2)

According to figure 1, in the equation *m* is *1* for upper HBCCs and *2* for lower HBCCs. Also *x* correspond with phase, namely *a*, *b, c*; and *n* for HBCCs connected to the neural network point. Minimum output voltage that an HBCC can produce is zero and maximum output voltage that an HBCC can produce is $V_{DC} = (n-1)V_{Cm}$. Therefore output voltage of an HBCC is always positive and the value of capacitor voltage of each HB inverter must be adjusted to below value:

$$V_{Cm} = \frac{V_{DC}}{(n-1)} \quad (2)$$

Due to the fact that each HBCC provides half of the current of corresponding phase, output voltages of upper and lower HBCCs are constantly in complementary form in every phase. In other words the total voltage of upper and lower HBCCs in each phase equals to V_{DC} at every instant, namely:

$$V_{x1} + V_{x2} = V_{DC} \quad (3)$$

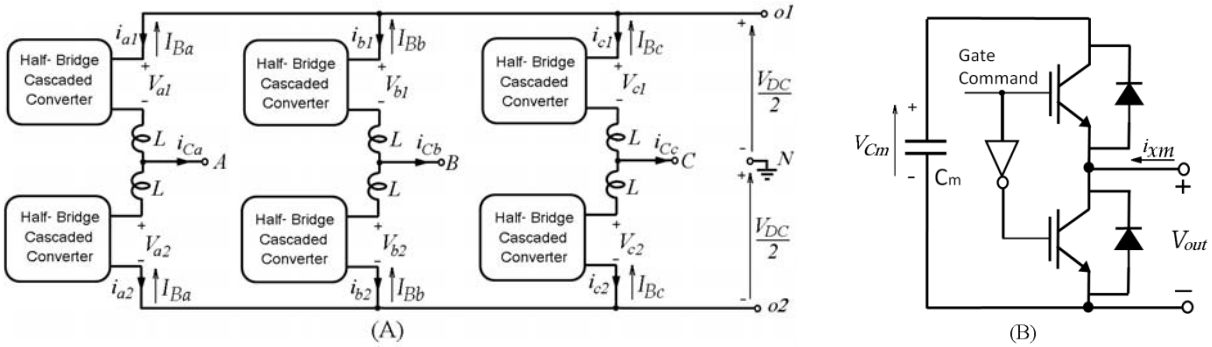

Fig. 2: (A) Description of three-phase three-wire HBCC based STATCOM topology, (B) Schematic of an HB inverter and its switches command

As a result, irrespective of the coupling inductors voltages, the voltage between upper and lower HBCC connection point ($V_{o1} - V_{o2}$) is always V_{DC}; while the voltage between the upper connection point (V_{o1}) and neural network point (V_N) is $V_{DC}/2$ and the voltage between the lower connection point (V_{o2}) and the neutral point (V_N) is $-V_{DC}/2$ as shown in figure 2(A).
When the converter provides unbalanced current to rebalance and compensate the nonlinear unbalanced load, one output terminal of the converter produces active power while the other terminals consume active power. It tends to reduce the capacitors' voltage of HBCCs that provide active power and increase the capacitors' voltage of HBCCs that consume active power. It further causes a direct current (I_B) flow from the HBCCs consuming active power part while providing active power to the HBCCs. Since upper and lower HBCCs in each phase leg provide or consume half of the active power of corresponding phase, magnitude of direct current in the upper HBCC (I_{Bx1}) is the same as magnitude of direct current in the lower HBCC (I_{Bx2}). In other words we have $I_{Bx1} = I_{Bx2} = I_{Bx}$. Under such circumstances, total current of each HBCC is equal to:

$$\begin{bmatrix} i_{x1} \\ i_{x2} \end{bmatrix} = \begin{bmatrix} \frac{i_{Cx}}{2} - I_{Bx} \\ -\frac{i_{Cx}}{2} - I_{Bx} \end{bmatrix} \tag{4}$$

The magnitude of balancing current I_{Bx} in each phase leg depends on the value of active power that will flow into or out of that phase leg. In realization of three or four legged converter, the sum of the total converter balancing currents will always be zero ($I_{Ba} + I_{Bb} + I_{Bc} + I_{Bn} = 0$). Therefore, electrical energy of all HBCCs remains balance. It is proved in the next part by equation (7). Because of the inductors in series with HBCCs, the increased current fluctuation of output converter currents can be damped substantially.
One of the advantages of the proposed compensator converter is that it can balance the network current in compliance with changes in load or even the impedance and the voltage of the network. The way through which voltages of all storage capacitors can be controlled is explained as follows.

Control

The controller of the proposed HBCC based STATCOM must perform the following major tasks:

1. Calculate proper output currents of the converter
2. Calculate reference voltage of the HBCCs
3. Generate switching signals and also
4. DC storage capacitors voltage balancing

The control system that accomplishes the above four tasks simultaneously is demonstrated here. We utilize the general instantaneous power theory [8] to calculate the current reference signals for each phase of the compensator as described in figure 3. The objective of this compensation theory is to make the currents of source completely sinusoidal, balanced and in phase with the first harmonic of positive sequence of source voltage. By having the voltage of point of common coupling (PCC) and

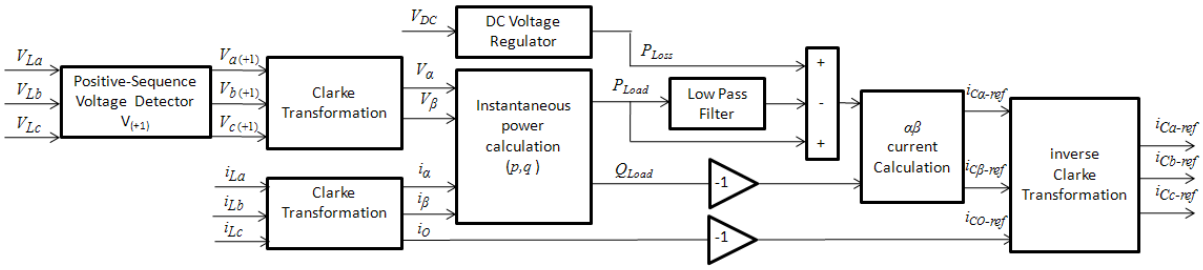

Fig. 3: The control block diagram for the sinusoidal current control strategy

reference current of compensator, the voltage of upper and lower HBCCs in each phase can be calculated as follows:

$$\begin{bmatrix} V_{x1} \\ V_{x2} \end{bmatrix} = \begin{bmatrix} \frac{V_{DC}}{2} - V_{Lx} - L\frac{di_{Cx}}{2dt} \\ \frac{V_{DC}}{2} + V_{Lx} + L\frac{di_{Cx}}{2dt} \end{bmatrix} \tag{5}$$

By a good approximation we write the above equation for a single switching period as:

$$\begin{bmatrix} V_{x1} \\ V_{x2} \end{bmatrix} = \begin{bmatrix} \frac{V_{DC}}{2} - V_{Lx} - \frac{L(i_{Cx(ref)} - i_{Cx})f_s}{2} \\ \frac{V_{DC}}{2} + V_{Lx} + \frac{L(i_{Cx(ref)} - i_{Cx})f_s}{2} \end{bmatrix} \tag{6}$$

In which i_{Cx} is the compensator current through phase *x* and $i_{Cx(ref)}$ is the current reference value of phase *x*, V_{x1} and V_{x2} are voltage references of upper and lower HBCCs in phase *x* respectively. V_{Lx} is the voltage of phase *x* in the point of common coupling. Also L is the amount of coupling inductance while f_s is the switching frequency of the converter.

There are several PWM modulation schemes that could be used with the half bridge cascaded converter. All these PWM modulation schemes have one thing in common. That is to say that each one of the switching commands is generated from the reference signal that is compared with a triangular carrier signal. The intersection points of these two signals will determine the commutation instants. In most cases, in order to achieve a multilevel output voltage, multicarrier PWM strategies are used, i.e., the carrier signals are independent and different in every complementary pair of semiconductors [12]. Therefore, each switching command has an independent carrier, but the reference signal could be shared between different pairs. The so-called "phase-shifted PWM" (PS-PWM) modulation technique as shown in figure 4 is one of these multicarrier PWM strategies, which is used in this paper.

In order to understand the voltage balancing of DC storage capacitors, let's analyze the modulation of one HB inverter while paying special attention to the DC-Bus capacitor current and the output voltage. As shown in figure 2(B), each HB inverter consists of a pair of complementary semiconductor branch connected to one DC-Bus. There are two different combinations depending on the individual switch that is switched on. Clearly, that if the upper switch is on, the output voltage of the inverter would equal to the DC-Bus voltage. In this condition, positive input current ($i_{xm} > 0$) would increase the voltage of the DC capacitor, while negative input current ($i_{xm} < 0$) would decrease the voltage of the DC capacitor. Also if the lower switch is on, the output voltage of the inverter would be zero while the capacitor voltage does not change. It is a very important conclusion that is used in the capacitor voltage balancing of an HBCC.

Thus, the following algorithm is introduced to balance the voltage of DC link capacitors of an HBCC:

- If the HBCC current is positive, then
  HB inverter with lower DC-Bus voltage level has to be switched on first.
- If the HBCC current is negative, then
  HB inverter with higher DC-Bus voltage level has to be switched on first.

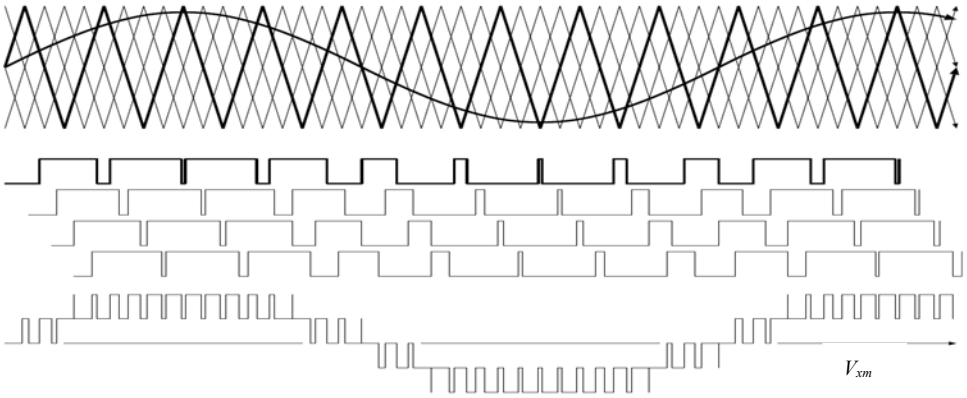

Fig. 4: Switching command generation in PS-PWM

According to (3), the modulation signals of upper and lower HBCCs in a phase are of complementary form, but the average active power of both are the same value. To prove this, we can adopt equations (4) and (5), to find the instantaneous power of each HBCC in a phase, as below:

$$\begin{bmatrix} P_{x1} \\ P_{x2} \end{bmatrix} = \begin{bmatrix} -\frac{V_{DC}}{2}(I_{Bx}) - (V_{Lx} + L\frac{di_{Cx}}{2dt}).(\frac{i_{Cx}}{2}) \\ -\frac{V_{DC}}{2}(I_{Bx}) - (V_{Lx} + L\frac{di_{Cx}}{2dt}).(\frac{i_{Cx}}{2}) \end{bmatrix} + \begin{bmatrix} (V_{Lx} + L\frac{di_{Cx}}{2dt}).(I_{Bx}) + \frac{V_{DC}}{2}(\frac{i_{Cx}}{2}) \\ -(V_{Lx} + L\frac{di_{Cx}}{2dt}).(I_{Bx}) - \frac{V_{DC}}{2}(\frac{i_{Cx}}{2}) \end{bmatrix} \quad (7)$$

During one network frequency cycle, the first terms of equation (7) have non-zero average values, while the second terms have zero average values. This is because the first terms of the equation are DC components while the second terms are AC components.

Thus, the average value of active power for upper and lower HBCCs in a single phase is identical; and hence DC capacitor voltage of the HB inverters of both is identical during one network frequency cycle. Due to non idealistic nature of HB inverters, the unbalance of the DC voltage in the upper and lower HBCCs can be eradicated through appropriate adjustment of reference current. In short, through utilization of above techniques, the voltage equality of all DC storage capacitors pertinent to the converter is assured.

To regulate the DC capacitors' voltage to a predetermined reference value, a DC voltage regulator unit is used in the reference current controller as depicted in figure 3. Therefore, the average of V_{DC} is compared with the reference value, and in accordance to their differences, the amount of total input or output active power of the compensator is obtained. It is clear that the value of this active power is equal to the converter power losses.

Simulation results

A $\pm 50MVA$ nine-level type of proposed HBCC-based transformerless STATCOM is simulated using PSIM and MATLAB-SIMULINK concurrently. Power circuit of the compensator is similar to that of figure 2(A). With regard to electrical railway application, the network phase voltage amplitude of 25kV is taken as an example. The simulated STATCOM contains six HBCCs, each of which is comprised of eight HB inverters in cascade. All the IGBTs have identical voltage and current ratings. The total number of IGBT modules used for the 25 kV STATCOM is 96 (= 6 × 8× 2). Each HB inverter has a DC storage capacitor with a nominal average DC voltage of 10 kV. The capacitance of DC storage capacitor in each HB inverter is determined on the basis of maximum permitted variations of DC voltage. This value can be calculated by the use of the following equation:

$$C_m \cong \frac{\int i_m(t).dt}{\Delta V_{Cm}} \quad (8)$$

In above equation, i_m is the instantaneous current passing through each of the HB inverters when we have highest fluctuation of load current, and ΔV_{Cm} is the maximum allowable voltage ripple for DC capacitors. Since the current controller momentarily adjusts the output current of the STATCOM,

variation of the DC links voltages in the permitted region will not cause chaotic state in the compensator operation.
Whenever we get abrupt changes in the load currents, the series coupling inductor (L), which is in series with each of the HBCCs of the converter damps the sudden rise of the balancing current I_{Bx}. It will also reduce the output current ripple of the STATCOM. The Inductance of all these inductors is identical and it is calculated according to maximum permitted ripple of an HBCC current. It can be calculated through the following equation:

$$L \cong V_{Cm}\frac{\Delta t}{\Delta i_m} = \frac{V_{DC}}{(n-1)}\frac{T_s}{\Delta i_m} = \frac{V_{DC}}{(n-1).f_s.\Delta i_m} \tag{9}$$

That Δi_m is the maximum allowable current ripple in all HBCCs. The PS-PWM modulation technique with a switching frequency of $f_s = 10$ kHz is applied to all HBCCs. The switching frequency is selected upon several factors such as switch types, level of output voltage and allowable THD content of output current.
Figure 5 shows voltage and current waveforms of the network, load currents, and compensator currents before and after compensation. Reference currents of each phase of converter has been set to zero before *t=0.1*Sec. Therefore load and source currents are similar during this period. Having activated the compensator, the source currents, comprising of load and compensator currents, are balanced to an acceptable value. In other words, source currents do not contain harmonics, while the load currents contain 10% third harmonic. In addition, source currents are in phase with the fundamental of positive sequence voltage and it doesn't contain reactive power components. As shown in figure 6, THD of source current is 1.14% which is compatible with IEEE and IEC standards.

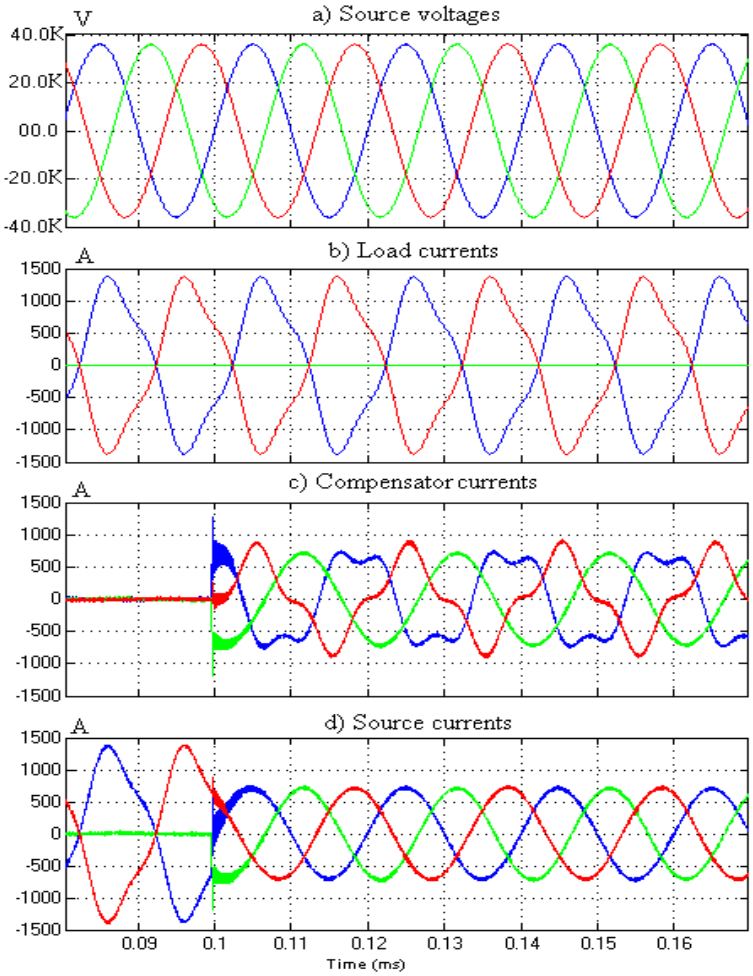

Fig. 5: Voltages and currents before and after compensation.

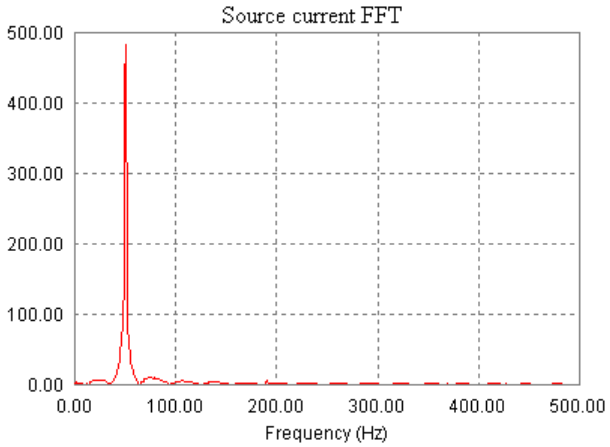

Fig. 6: FFT spectrum of source current after Compensation (THD < 1.14)

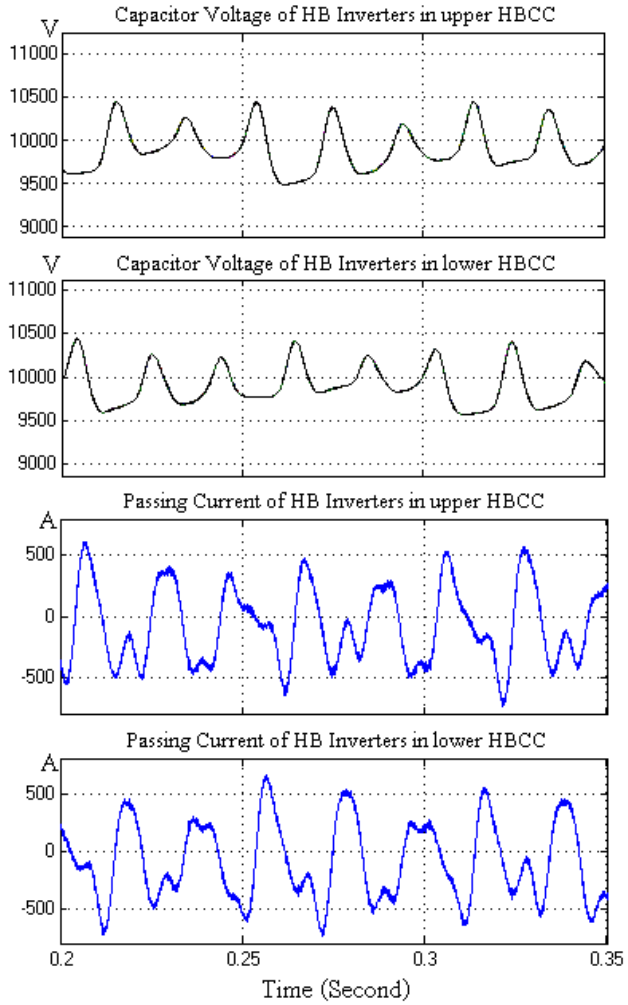

Fig. 7: Capacitor voltages and passing current of HB inverters of upper and lower HBCC in phase *a*

The compensator absorbs active power by one phase and injects it to other phases, while its DC capacitors' voltages are regulated according to the reference value. Figure 7 shows DC storage capacitor voltage and output currents of each HB inverter for upper and lower HBCCs in phase A. When the output currents of the compensator tend to become unbalanced, the magnitude of HBCCs' currents will increase. In worst conditions, the peak instantaneous HBCCs' currents become equal to the maximum output current of the compensator. This is due to presence of balancing currents in the

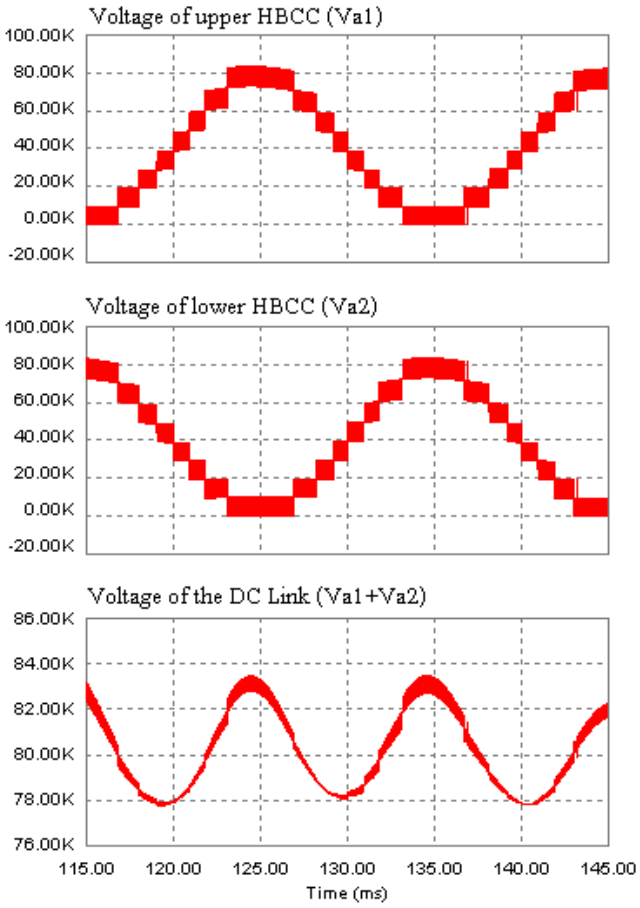

Fig. 8: Voltages of upper and lower HBCCs in phase *a* and the sum of them (V_{DC})

compensator loops. As the magnitude of load current unbalance decreases, the magnitude of balancing currents will decrease accordingly.

Figure 8 shows voltage waveforms of upper and lower HBCCs of the converter in phase *a*. As it can be seen, the sum of upper and lower HBCCs' voltage in each phase is held at V_{DC} while the voltage of one HBCC varies from zero to V_{DC}. Neglecting the inductor voltage of each HBCC, the voltage between converter phases and neutral point of network will vary from $V_{DC}/2$ to $-V_{DC}/2$, while the line voltage of converter varies from V_{DC} to $-V_{DC}$ during each cycle of network frequency.

On the other hand, as the sum of voltages of upper and lower HBCCs deviate from V_{DC}, a current will flow from higher voltage HBCCs to lower voltage HBCCs to reduce this difference. The magnitude of this current depends on voltage difference between upper and lower HBCCs. When these currents start to flow, active power will inevitably flow between the compensator phases.

Conclusion

In this paper a novel topology has been proposed to compensate the unbalanced and nonlinear medium voltage loads under presence of load and source harmonics. The main advantage of this topology is its modularity, compatibility of operation under nonlinear conditions and its ability to work without any low frequency transformer.

Various modular topologies with isolated DC link have been proposed such as cascaded converters with delta or Y connections. But they cannot compensate unbalanced loads with harmonic contents either delta, Y or both. In fact cascaded converters with delta connection cannot possibly inject third harmonic current or compensate neutral current. In Y connected cascaded converters, rebalancing of unbalanced loads is done with some problems. Injection of unbalanced currents by this converter causes injection of active power with non-zero average magnitude from each phase. This will in turn, makes controlling of DC storage capacitor voltages almost impossible.

The proposed modular converter is the developed model of cascaded converter with Y connection that utilizes several isolated units. Each unit comprises a half-bridge-inverter linked to isolated DC capacitors. By utilization of aforementioned controller (part III), all DC capacitors' voltages will be adjusted to a predetermined magnitude. Simulation results prove proper operation of the converter under unbalanced-harmonic conditions.

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