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Efficiency of three-level neutral-point clamped converters: analysis and experimental validation of power losses, thermal modelling and lifetime prediction

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Abstract: Multilevel converters are growing fast, whereas industry needs particular tools to evaluate efficiency and performance of such converters. This study focuses on the analysis and practice of power losses in a three-level neutral-point clamped (NPC) inverter. First, a precise mathematical model for three-level inverters is introduced to be used for simulating power losses of the switches, providing AC voltage and current of each phase, voltage and current of the switches as well as both the conduction and switching losses. Further, an NPC inverter was developed to validate the analytical work by comparing experimental results with those of simulations. Additionally, the thermal modelling of semiconductors is obtained using datasheet parameters. Then, the temperature rise is further modelled using the power losses along with the thermal model in the form of *RC* ladder. Finally, the lifetime of semiconductors is predicted using the heating curves in line with the power-cycling concept. The measured power losses and temperatures in comparison with the presented model suggest this kind of research as an applicable replacement for expensive measuring devices.

1 Introduction

In recent years, renewable energy sources such as wind turbines, photovoltaic systems or biogas plants have become increasingly important. In the meantime, the point of common coupling is shifting from low voltages to medium voltages because of the growing power ratings by the producers. These medium voltage inverters could perform under lower switching frequencies to reduce the switching losses. However, the quality of the output voltage is affected by high amplitude low order harmonics. This causes additional harmonic losses as well as higher total harmonic distortion (THD). Considering these reasons, analysis and estimation of power losses and temperature rise in multilevel converters have several benefits such as optimal heatsink size design, thermal stress evaluation and semiconductor aging prediction, in line with improving both the performance and reliability in designing power converters. For example industrial sectors, such as smart grids an active network, are willing to employ high quality multilevel converters because of their low THD. Hence, condition monitoring and lifetime prediction would be necessary for optimal design of medium voltage converters more than ever.

In general, power losses in semiconductor switches are divided into two groups; conduction losses and switching losses. On-state power losses, when the insulated-gate bipolar transistor (IGBT) is completely on, can be described by a simple model; a voltage source drop (u_{CE0}) that represent on-state zero-current emitter–collector voltage in series with a resistor (r_C). Similarly, u_{D0} and r_D represent the conduction model for a diode. Thus, the average conduction losses for both the IGBT (P_{CT}) and diode (P_{CD}) are presented as below

$$\begin{cases} P_{CT} = u_{CE0} I_{Cav} + r_C I_{Crms}^2 \\ P_{CD} = u_{D0} I_{Dav} + r_D I_{Drms}^2 \end{cases} \quad (1)$$

where I_{Cav} and I_{Dav} are the average IGBT and diode currents, I_{Crms} and I_{Drms} are the RMS values of IGBT and diode currents, P_{CT} and P_{CD} are the average power losses of the IGBT and diode, respectively [1]. Note that parameters like u_{CE0} and r_C as well as u_{D0} and r_D can be obtained from their corresponding datasheets [2].

Real switches also introduce switching power losses during both turn on and turn off; in particular, reverse recovery diodes should be taken into account [3, 4]. Switching losses can be mathematically modelled and analysed accurately [5–7]; but transition of current and voltage waveforms differ from one IGBT to another. Therefore it is unrealistic to introduce a general formulation for calculation of switching losses. Nonetheless, using the curves of 'switching energy losses against current' and 'switching energy losses against gate resistance R_G' could be helpful to

approximate switching losses (these are also included in datasheets). In addition, switching losses depend on DC-link voltage V_{DC} and junction temperature of semiconductor T_j. Normalising these parameters by a reference value specified in datasheet, the following formula is obtained

$$E_{on} = (A_{on}I_C + B_{on})\frac{E_{on}(R_G)}{E_{on}(R_{G,datasheet})}\frac{V_{DC(on)}}{V_{DC,datatsheet}}\frac{E_{on}(T_j)}{E_{on}(T_{j(max)})} \quad (2)$$

where A_{on} and B_{on} are obtained from linear interpolation of the energy losses against current of the IGBT (I_C), both $E_{on}(R_G)$ and $E_{on}(R_{G,\,datasheet})$ are obtained from energy losses against gate resistor of IGBT, $V_{DC(on)}$ is half of V_{DC}, $E_{on}(T_j)$ are the energy losses at the operating temperature and maximum operating temperature of IGBT, respectively. Similar relationship is derived for E_{off} [8]. Adding the turn-on energy losses (E_{on}) to the turn-off energy losses (E_{off}) in one 'fundamental period' gives the total switching power losses (P_{SW}) of the IGBT as below

$$P_{SW} = (E_{on} + E_{off})f_{fundamental} \quad (3)$$

where $f_{fundamental}$ is the fundamental frequency of the output voltage. Here a software was developed in which both the turn-on and turn-off energy curves are interpolated. Additionally, since the provided curves are dedicated to a specific gate resistor, DC-link voltage and junction temperature, some modifications and formulations were arranged by using other useful curves from datasheet. These extensions show energy losses against gate resistance and junction temperature, paving the way for calculating switching losses by software.

Calculation of power losses have already been studied in many literatures. In [9, 10], a mathematical model is used to work out the power losses. In [11, 12], dynamic thermal parameters of semiconductors are calculated through datasheet and/or experiments, providing temperature rise of the connection point. Also, long-term experiments are reported in [13–15] in which the switching packages are subjected to thermal stress. The junction temperature rise is then used to obtain the average temperature as well as the difference between maximum and minimum junction temperature. Long-term experiments are reported in [5–7] in which switching modules were subjected to thermal stress. Then, the lifetime of semiconductor was predicted according to the temperature rise of connecting point of the modules as well as statistics models. These kinds of literatures normally concentrate on lifetime prediction using probabilistic approach rather than accurate power loss and temperature rise.

This paper concentrates on calculation of the exact power losses of a three-level inverter by numerical methods, both for the conduction and switching intervals. A mathematical model is developed to calculate the needed currents and voltages of three-level inverter accurately. Then, the temperature rise is estimated for semiconductor switches using the calculated power losses. Furthermore, heating curve of semiconductor switches is used to predict their lifetime by employing the power-cycling concept. To verify the introduced analysis, a 6 kVA three-level diode-clamped inverter was used in experimental evaluation of power losses. The DSPTMS320F28335 was used to modulate and control of the three-level inverter. To verify the performed investigations, it is necessary to measure junction temperatures of switching devices. This cannot be fulfilled by usual thermometers in practice. A thermo-vision camera was employed to do so. In brief, comparing the experimental results with those of simulations confirms the performed analysis and theoretical discussions.

2 Modelling the three-level inverter

It is necessary to model three-phase inverters to obtain voltage and current waveforms for each element like IGBT and diode, working out the power losses accurately. There exist two ways in modelling a converter; first, the whole inverter is simulated by a real-time software (e.g. PSPICE). Second, the inverter is modelled analytically using differential equations, where the resultant outcome needs to be developed by software. Fig. 1*a* shows a three-level inverter that is further introduced by a simplified single pole triple throw (SPTT) equivalent circuit for phase *a* in Fig. 1*b*. Here the SPTT acts as an ideal switch, V_a is the output voltage for phase *a*, V_L and I_L are the inductor

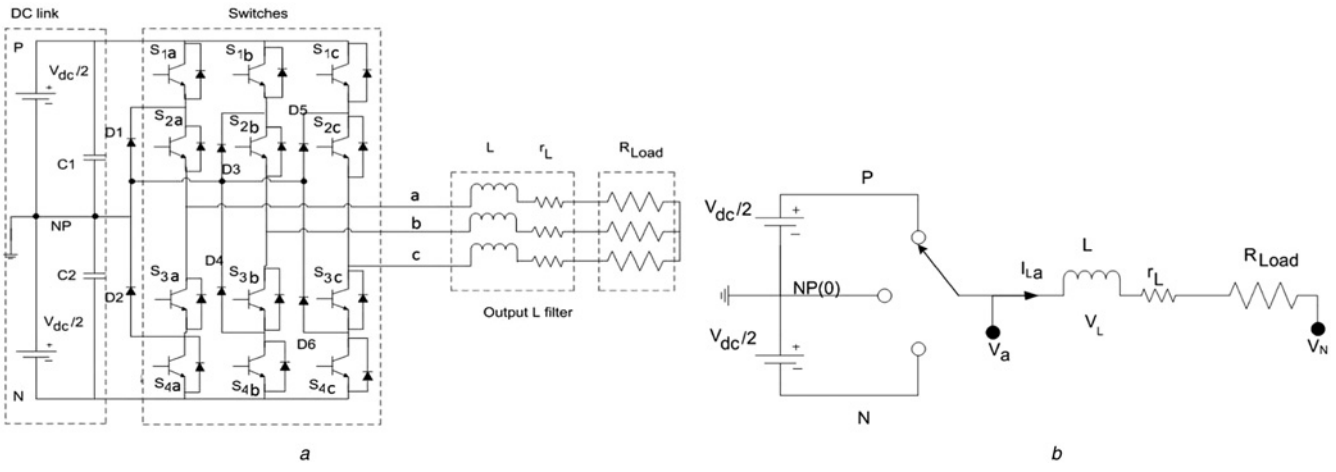

Fig. 1 *Modelling the three-level inverter*

a Three-level diode clamped inverter supplying a load through a low-pass *RL*-filter
b Simplified equivalent circuit of the three-level inverter of Fig. 1 for phase *a*

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voltage and current, L is the AC-side filter inductance, r_L is the winding resistance related to the inductance L, R_{load} is the load resistance and V_{N} is the neutral point (NP) voltage. Starting from $V_{j=a,\ b,\ c}$, a KVL can relate V_j to V_{N} as below

$$V_j = L\frac{\mathrm{d}I_{Lj}}{\mathrm{d}t} + I_{Lj}r_L + I_{Lj}R_{\text{Load}} + V_{\text{N}}, \quad (j = a, b, c) \tag{4}$$

Also, the neutral point voltage can be related to the phase voltages in three-phase systems

$$V_{\text{N}} = (V_a + V_b + V_c)/3 \tag{5}$$

Combining (4) with (5) as well as doing further rearrangement for getting two independent inductor currents leads to

$$\begin{cases} \dfrac{\mathrm{d}I_{La}}{\mathrm{d}t} = -\dfrac{I_{La}(r_L + R_{\text{Load}})}{L} + \dfrac{1}{3L}(2V_a - V_b - V_c) \\ \dfrac{\mathrm{d}I_{Lb}}{\mathrm{d}t} = -\dfrac{I_{Lb}(r_L + R_{\text{Load}})}{L} + \dfrac{1}{3L}(2V_b - V_a - V_c) \end{cases} \tag{6}$$

where instant values of V_a, V_b and V_c depend on the position of the SPTT of each phase.

2.1 Switching modelling

The inverter leg a is composed of four active switches S_1–S_4 (IGBT) with four anti-parallel diodes. Here each two pairs (S_1, S_3) and (S_2, S_4) are complementary switched, connecting each phase to three voltage levels $V_{\text{DC}}/2$, 0, $-V_{\text{DC}}/2$ with respect to ground (see Fig. 1). Thus, the phase voltages can be described as follows

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} S_{1a}S_{2a} - S_{3a}S_{4a} \\ S_{1b}S_{2b} - S_{3b}S_{4b} \\ S_{1c}S_{2c} - S_{3c}S_{4c} \end{bmatrix} \frac{V_{\text{DC}}}{2} \tag{7}$$

Substituting (7) in (6) results in the following non-linear time-dependent state space equations (see (8))

where $\boldsymbol{X}$ is the state vector, u is the input DC voltage, $\boldsymbol{A}$ is the state matrix and $\boldsymbol{B}$ is the input coefficients matrix. Solving (8) needs finding input matrix $\boldsymbol{B}$, that depends on switching functions. Thus, the converter time-dependent model is a variable structure system which should be solved N switching times over a given fundamental period T

$$\sum_{i=1}^{i=N}(t_{i+1} - t_i) = T \tag{9}$$

where t_i and t_{i+1} are the ith two consecutive switching instants in which state equations are solved (i.e. N various set of state equations have to be solved).

2.2 Solving the equations by numerical method

Solving the nonlinear differential state equations (8), in combination with (9), should be fast in order to be applied in real-time power losses calculations such as estimation of switching module temperature. Hence, numerical methods in discrete domain can be nominated to do so. Here a program was developed for the three-level inverter to work out the model described by (8) followed by calculations of power losses. First, a general SPWM modulation technique was programmed, calculating the switching edges t_i. Then, the calculated switching values at the obtained switching edges are replaced in (8) to obtain the discrete form of (8) as (see (10))

3 Dynamic thermal modelling

Reliability and lifetime prediction of power electronic component strongly depend on calculation of exact power losses as well as accurate computation of thermal stress. A dynamic electro-thermal model of the semiconductor switch (e.g. IGBT) and the applied heatsink is necessary for calculating thermal stress. Thermal model of various materials is composed of equivalent RC-networks, generally described by Foster and Cauer [16]. Fig. 2a shows a fourth-order Cauer model for an neutral-point clamped (NPC) module including IGBT, freewheel diode and clamping diode. Equivalent impedance of the junction to

$$\begin{aligned} &\dot{\boldsymbol{X}} = \boldsymbol{A}\boldsymbol{X} + \boldsymbol{B}u, \quad \text{where} \\ &\boldsymbol{X} = \begin{bmatrix} I_{La} \\ I_{Lb} \end{bmatrix},\ u = V_{\text{dc}}, \quad \boldsymbol{A} = \begin{bmatrix} (r_L + R_{\text{Load}})/L & 0 \\ 0 & (r_L + R_{\text{Load}})/L \end{bmatrix} \\ &\boldsymbol{B} = \frac{1}{6L}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix}\begin{bmatrix} S_{1a}S_{2a} - S_{3a}S_{4a} \\ S_{1b}S_{2b} - S_{3b}S_{4b} \\ S_{1c}S_{2c} - S_{3c}S_{4c} \end{bmatrix} \end{aligned} \tag{8}$$

$$\begin{aligned} \begin{bmatrix} I_{La}(i) \\ I_{Lb}(i) \\ I_{Lc}(i) \end{bmatrix} &= \left(1 - \Delta t\frac{(r_L + R_{\text{Load}})}{L}\right)\begin{bmatrix} I_{La}(i-1) \\ I_{Lb}(i-1) \\ I_{Lc}(i-1) \end{bmatrix} + \frac{V_{\text{dc}}}{6L} \\ &\times \left(2\begin{bmatrix} S_{1a}S_{2a} - S_{3a}S_{4a} \\ S_{1b}S_{2b} - S_{3b}S_{4b} \\ S_{1c}S_{2c} - S_{3c}S_{4c} \end{bmatrix}_{(i-1)} - \begin{bmatrix} S_{1b}S_{2b} - S_{3b}S_{4b} \\ S_{1c}S_{2c} - S_{3c}S_{4c} \\ S_{1a}S_{2a} - S_{3a}S_{4a} \end{bmatrix}_{(i-1)} - \begin{bmatrix} S_{1c}S_{2c} - S_{3c}S_{4c} \\ S_{1a}S_{2a} - S_{3a}S_{4a} \\ S_{1b}S_{2b} - S_{3b}S_{4b} \end{bmatrix}_{(i-1)}\right) \end{aligned} \tag{10}$$

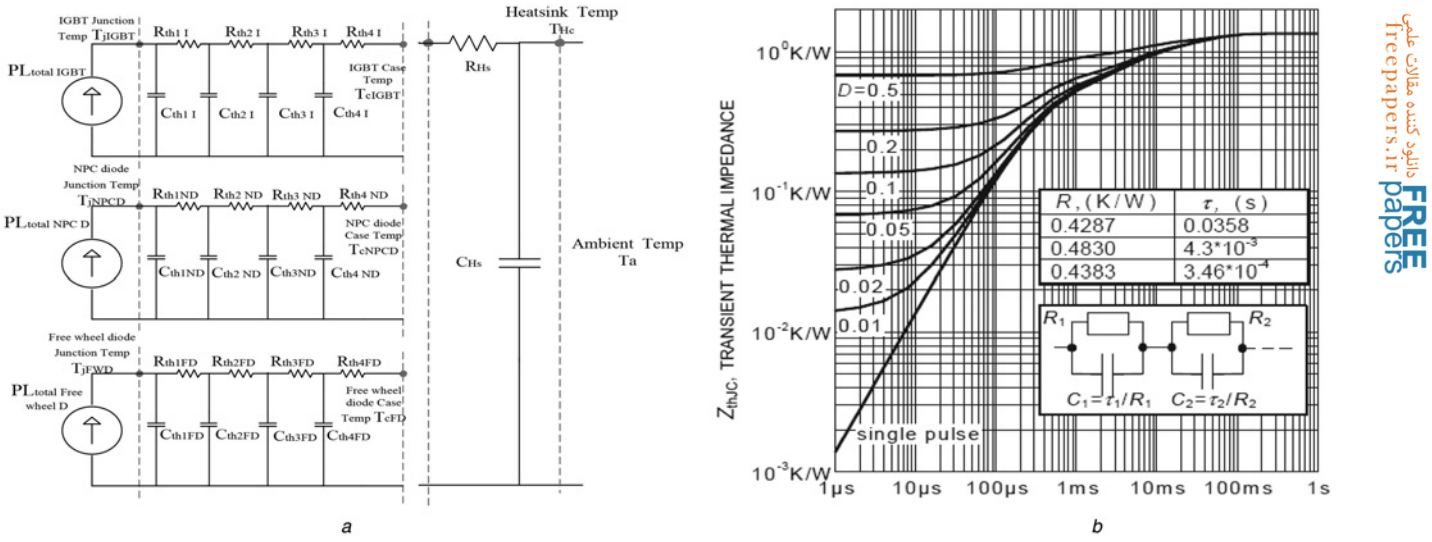

Fig. 2 *Dynamic thermal modelling*

a Cauer thermal model of freewheel diode, clamping diode and IGBT mounted on heatsink
b Junction to case thermal impedance of IGBT (Foster model) [2]

heatsink (Z_{thJH}) can be calculated as below [17]

$$Z_{thJH} = \cfrac{1}{sC_1 + \cfrac{1}{R_1 + \cfrac{1}{sC_2 + \cfrac{1}{R_2 + \cfrac{1}{sC_3 + \cfrac{1}{R_3 + \cfrac{1}{sC_4 + \cfrac{1}{R_4}}}}}}}} \tag{11}$$

where the unknown parameters, like R_i and C_i, can be obtained from the module datasheet. Resistances R_i can be directly read, whereas capacitances C_i should be computed from the given $\tau_i = R_i C_i$. It should be noted that these extracted parameters are suitable for Foster model in IGBT datasheets as shown typically in Fig. 2*b*; further adaptation will be required for the Cauer model by computing the equivalent input impedance Z_{in} at different stages using denominator divided by numerator continuously [17].

Table 1 lists typical Foster and Cauer thermal impedances obtained from an IGBT datasheet. The obtained values for the resistors and capacitors are then substituted in Cauer model (11) to obtain the thermal input impedance transfer functions for both IGBT (including its freewheeling diode) and clamping diode as below

Three transient responses can be seen in Fig. 3*a* that describes the behaviour of three transfer functions related to

Table 1 Obtained Cauer and Foster parameters from datasheet

Parameter	Cauer	Foster
R_1	0.5248	0.4287
R_2	0.5044	0.4830
R_3	0.3208	0.4383
C_1	0.00071	0.0835
C_2	0.0087	0.0089
C_3	0.1008	0.00078

the IGBT (switches S_1 and S_2) and clamping diode using (12). The ripple of heating curve for each semiconductor device can be used for calculating the thermal stress of the whole module.

Thus, the developed software is used to work out the instantaneous power losses of each semiconductor device, where P_{IGBT} stands for both the IGBT and the freewheel diode. These powers can be multiplied by the obtained transfer function in (12) to obtain the temperature rise. Furthermore, in [18], superposition is suggested for calculating the temperature rise in a complete device ($\Delta T_{IGBTFD.JC}$) as below

$$\Delta T_{\text{IGBTFD JC}} = Z_{\text{th jH IGBT}}\, P_{\text{IGBT}} \tag{13}$$

where $\Delta T_{IGBTFD.JC}$ is temperature rise of both the IGBT and freewheel diode. In addition, thermal conductivity of the experimental NPC inverter uses naturally cooled heatsink. The thermal resistance of heatsink could be found in datasheet published by manufacturer or is calculated according to the size and shape of heatsink. A small aluminium heatsink with five fins is used to take the heat

$$\begin{cases} Z_{\text{th jC IGBT}}(s) = \dfrac{7.409e-5\,s^2 + 0.03703\,s + 1.35}{5.326e-8\,s^3 + 0.0001678\,s^2 + 0.04045\,s + 1} \\ Z_{\text{th jC Diode}}(s) = \dfrac{7.214e-8\,s^3 + 0.0003087\,s^2 + 0.09993\,s + 2.4}{6.596e-12\,s^4 + 1.296e-7\,s^3 + 0.00026\,s^2 + 0.06\,s + 1} \end{cases} \tag{12}$$

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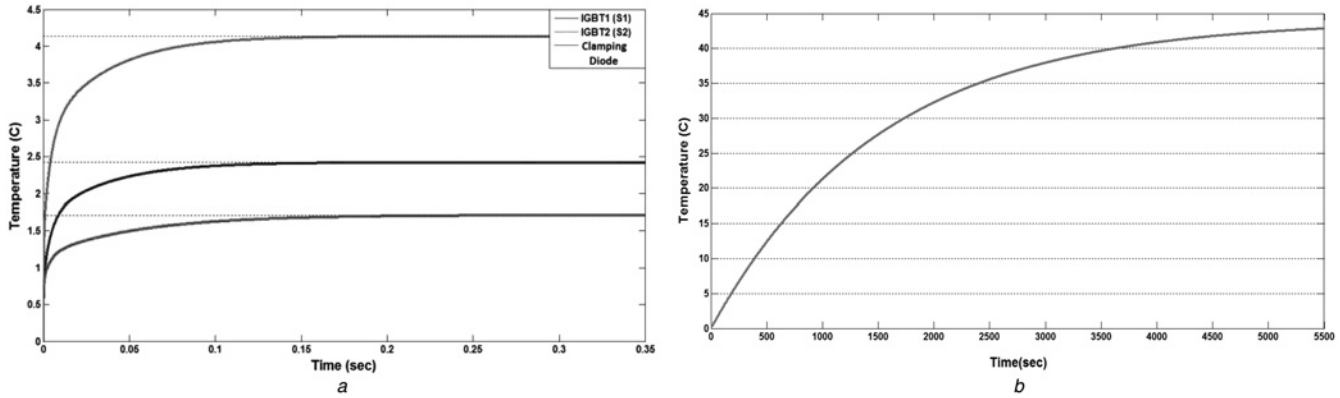

Fig. 3 *Three transient responses*

a Junction-case temperature rise of IGBT and diode (ΔT_{JC})
b Heatsink temperature rise (ΔT_{HA})

from semiconductors. Sill-pad with silicon grease is used for electrical insulation of attached IGBTs to the heatsink. Also, the thermal resistance of insulator ($Z_{\text{th CH IGBT}}$) should be considered for accurate thermal model of inverter. The range of resistance for sill-pad and silicon grease varies within 1.5–1.7°C/W according to the application notes.

Several methods are presented in [19–21] that can be used for calculating the thermal resistance of heatsinks. The data of thermal impedance of heatsink was calculated, where Fig. 3*b* shows the response of heatsink (heatsink-to-ambient temperature rise ΔT_{HA}). Comparing thermal response of heatsink with those of the switches (see Fig. 3*a*) shows much faster response for semiconductors because of their huge differences in both material and size. Since the IGBTs are mounted on heatsink, total power losses (P_{total}) are multiplied by the heatsink transfer function ($Z_{\text{th HA}}$) to obtain ΔT_{HA}. Hence, for example temperature of an IGBT junction including the freewheeling diode ($T_{\text{IGBTFD j}}$) can be calculated by adding its junction-to-ambient temperature rise ($\Delta T_{\text{IGBTFD jA}} = \Delta T_{\text{IGBTFD jC}} + \Delta T_{\text{IGBTFD CH}} + \Delta T_{HA}$) to the ambient temperature T_{Amb} as follows

$$T_{\text{IGBTFD j}} = \overbrace{Z_{\text{th jC IGBT}} P_{\text{IGBT}}}^{\Delta T_{\text{IGBTFD JC}}} + \overbrace{Z_{\text{th CH IGBT}} P_{\text{IGBT}}}^{\Delta T_{\text{IGBTFD CH}}} + \overbrace{Z_{\text{th HA}} P_{\text{total}}}^{\Delta T_{HA}} + T_{\text{Amb}} \quad (14)$$

4 Lifetime prediction

The power cycle test (PCT) is among the main models that used in reliability and lifetime prediction of semiconductors. Principles of the PCT are based on applying power dissipation pulses to a switching module, measuring voltage and current of the collector–emitter. Then, the number of cycles-to-failure N_f can be approximated. Fig. 4*a* shows power cycles in one period of fundamental frequency, that is applied to the dynamic thermal model of switching components in order to simulate the transient thermal stress. This experiment is repeated several times, where Weibull statistical analysis on results of power cycle will approximate N_f as below [22]

$$N_f = A\Delta T_j^{\alpha} e^{(E_a/K_B T_m)} \quad (15)$$

where ΔT_j is the difference between maximum and minimum junction temperatures, T_m is the average of maximum and minimum junction temperatures in Kelvin, $K_B = 1.38 \times 10^{-23}$ is the Boltzmann constant, and $E_a = 9.89 \times 10^{-20}$ J is the activation energy, $A = 310$ and $\alpha = -5$. These parameters are valid for IGBT modules and for other types of semiconductors power cycling tests should be repeated.

It can be seen from (15) that the lifetime depends on ΔT_j^{α} such that the higher this thermal stress, the lower the life of semiconductors [22, 23]. Fig. 4*b* shows a typical junction temperature oscillations for an IGBT, where minimum and

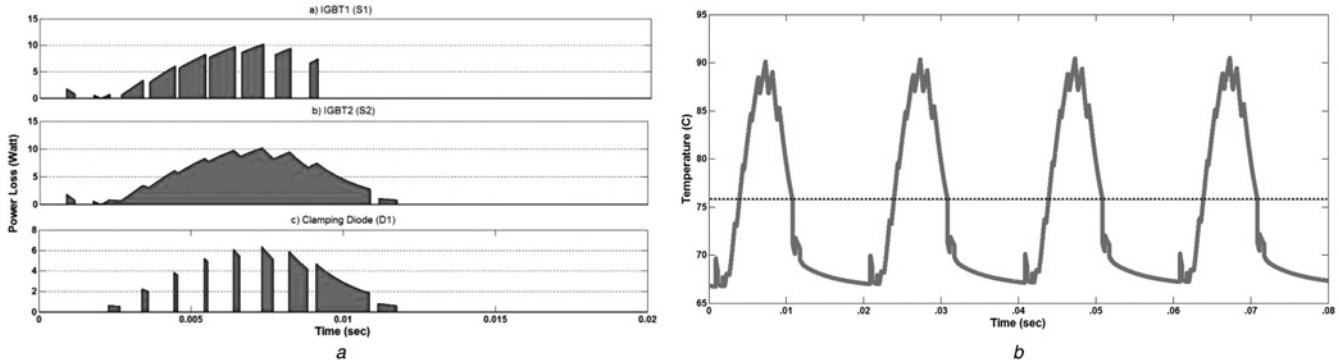

Fig. 4 *Power cycle test*

a Power loss cycles of semiconductors during one period of fundamental frequency
b Transient Junction temperature of IGBT ($T_{\text{J IGBT}}$)

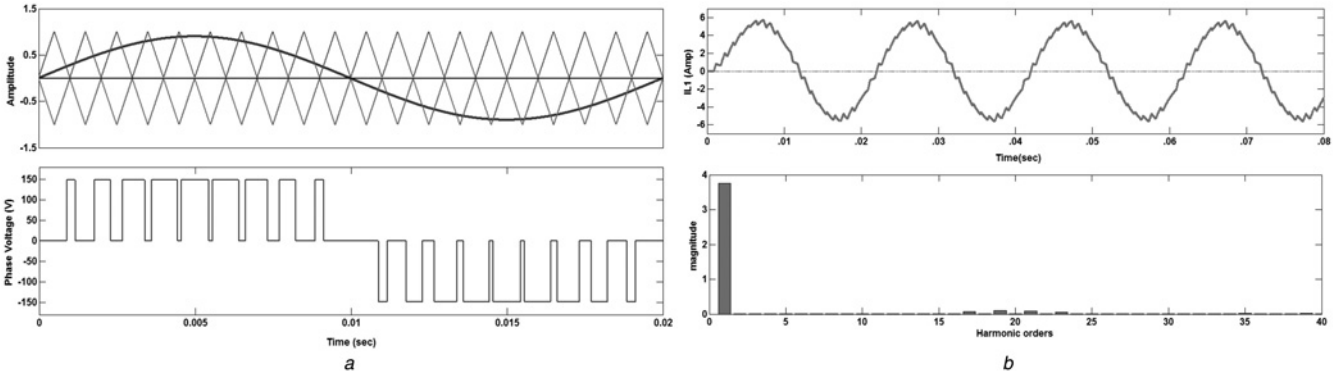

Fig. 5 *Simulation using the developed software*

a The SPWM with a 1 kHz triangular carrier for three-level inverter
b Inverter current at phase *a* along with its Fourier transform for harmonics content by the developed program

maximum as well as the average junction temperatures (67°C, 90°C and 76°C, respectively) can be calculated using this thermal curve. Replacing these parameters in (15) results in $N_f = 4.76 \times 10^8$. In fact, under these power cycles condition, the likelihood of failure in the semiconductor module significantly increases.

5 Simulations using the developed software

Assume the well-known SPWM modulation technique is applied to the NPC three-level converter as shown in Fig. 5*a*. The developed software is composed of four parts that are operating as a unit program: (a) switching angle generator block, which calculates switching angles according to the frequency and switching strategy, (b) power losses (conduction and switching) calculation based on current, voltage, temperature and electrical parameters of IGBT, (c) temperature unit that calculates temperature rise of switches based on power losses and thermal parameter of semiconductors and (d) lifetime prediction based on power cycles and temperature variations. First, the PWM that generates switching instants. The phase and line voltages can be easily modulated using these switching angels along with DC-link voltages and modulation indexes (see Fig. 5*a*). Second, phase voltages are used to solve (10) in discrete domain, calculating three-phase current waveforms. The current for phase *a*, including its harmonic content, is shown in Fig. 5*b*. Third, both conducting and switching losses are programmed using the generated currents and voltages of the mentioned parts together with the parameters extracted from datasheet. The final part works out dynamic temperature curve of each switch by applying the power losses to the total thermal transfer function of the module and semiconductor switches described in Section 4.

Figs. 5 and 6 describe the resulting output waveforms by the developed software when parameters of Fig. 1 are chosen as $V_{DC} = 300$ V, $L = 0.063$ H, $r_L + R_{load} = 21\ \Omega$, $f_s =$ 2 kHz (carrier frequency) and $m_a = 0.9$ (modulation index). Fig. 6 introduce simulated currents of switches located at phase *c* of the three-level converter based on current and voltage of phase *c*. These switch currents along with r_C, r_D, v_{ce0} and v_{d0} can be applied to the procedure explained in Section 2 to calculate conduction losses. The developed program is also capable of providing accurate switching angels for each switch and its current at that switching

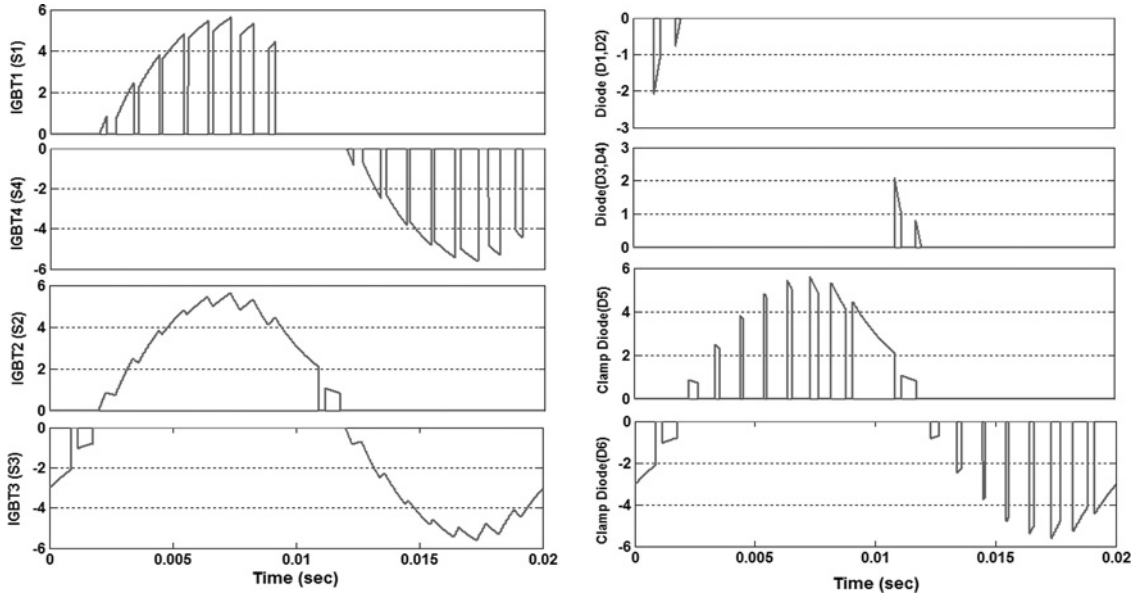

Fig. 6 *Current calculation for each switch using the developed program*

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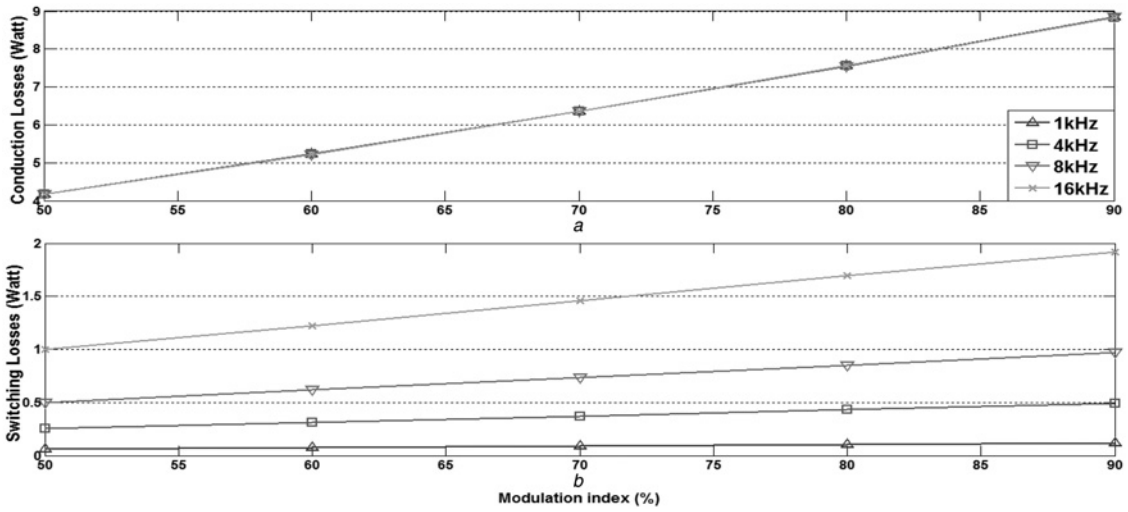

Fig. 7 *Conduction and switching power losses*

a Comparison among calculated conduction power losses for four-carrier frequencies
b Comparison among calculated switching power losses for four-carrier frequencies

instant. Thus, energy losses can be calculated using the energy against current chart, current at the switching time, R_G, V_{DC} and T_j as stated in (3). The switching power losses can then be found using the calculated energy losses and fundamental frequency as follows

$$P_{\text{swtotal}} = (E_{\text{on}} + E_{\text{off}} + E_{\text{offd}}) f_{\text{fundamental}} \tag{16}$$

where E_{offd} is the freewheeling diode turn-off energy loss. Here conduction and switching losses is calculated for four switching frequencies 2, 4, 8 and 16 kHz. Fig. 7*a* compares conduction losses in various switching frequencies against different modulation indexes. It can be seen that increasing the switching frequency somehow decreases conduction losses because of lowering harmonic currents. Further, switching losses are significantly increased by switching frequency as shown in Fig. 7*b*.

6 Experimental results

Here the outcomes of the developed program, stated in Section 5, is compared with those of an implemented three-level inverter. The practical work was arranged on a three-level NPC using 'SKP10N60A' IGBT [2] for three-phase switches. A two-layer circuit board was designed for installing gate drivers, and a three-phase rectifier connected to an auto-transformer used as the DC-supply. Four IGBTs and two diodes are located on a heatsink for each phase, and then heatsinks screwed on a board. Fig. 8*a* shows the complete inverter circuit that is connected to the three-phase load. Regarding the load, an *RL* arrangement was connected to the three-level inverter, having parameter values of $L = 63$ mH and $R = 21\ \Omega$; a SPWM with 2 kHz carrier frequency used as switching modulation technique, where the experiments were performed for modulation indexes in the range of 50–90%.

Moreover, the DSP TMS320F28335 was used for generating switching pulses in various frequencies and modulation indexes. Also, a power analyser, as shown in Fig. 8*b*, were connected to the three-level inverter for measuring the power losses. The power analyser was connected to the DC-link and output phases for measuring the input and output power. Thus, the experimental results can be compared with those of the programmed simulations correspondingly.

6.1 Power loss measurements

First, developed mathematical model (8)–(10) are examined. Various experiments were compared with outcomes of the simulated software in order to confirm the suggested model. Here it is presented typical experiments that measure four resultant phase currents and voltages at 2, 4, 8 and 16 kHz as shown in Figs. 9*a–d*.

Then, the measured power losses from the practical work were gathered for various modulation indexes under various switching frequencies. Figs. 10*a–d* present the power losses simulated at 2, 4, 8 and 16 kHz by the developed software in comparison with their corresponding experiments. It is

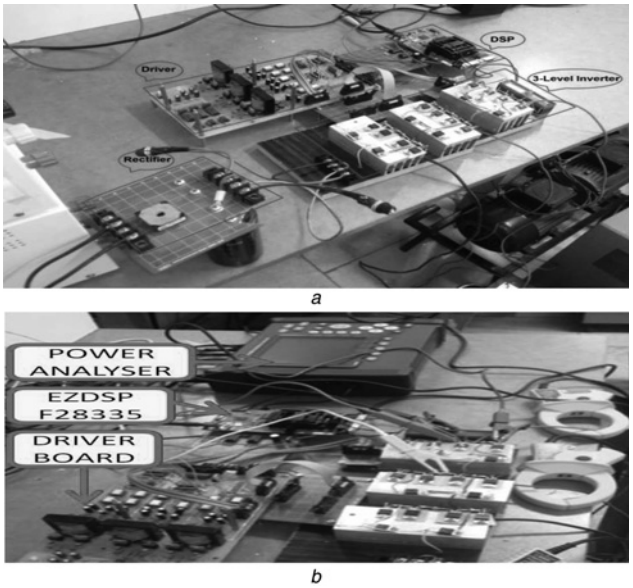

Fig. 8 *Inverter circuit and power analyser*

a Various circuit boards of the implemented three-level inverter
b Power analyser measuring DC and AC sides of the inverter

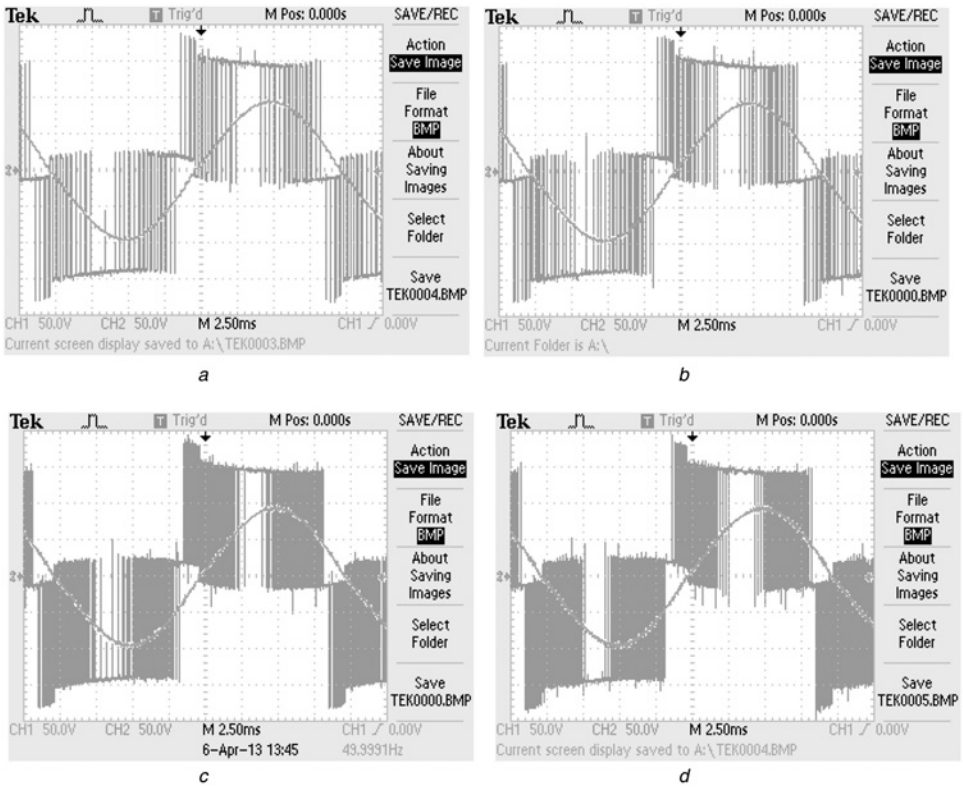

Fig. 9 *Measured phase current and voltage at modulation index 90% when carrier frequency*

a 2 kHz
b 4 kHz
c 8 kHz
d 16 kHz

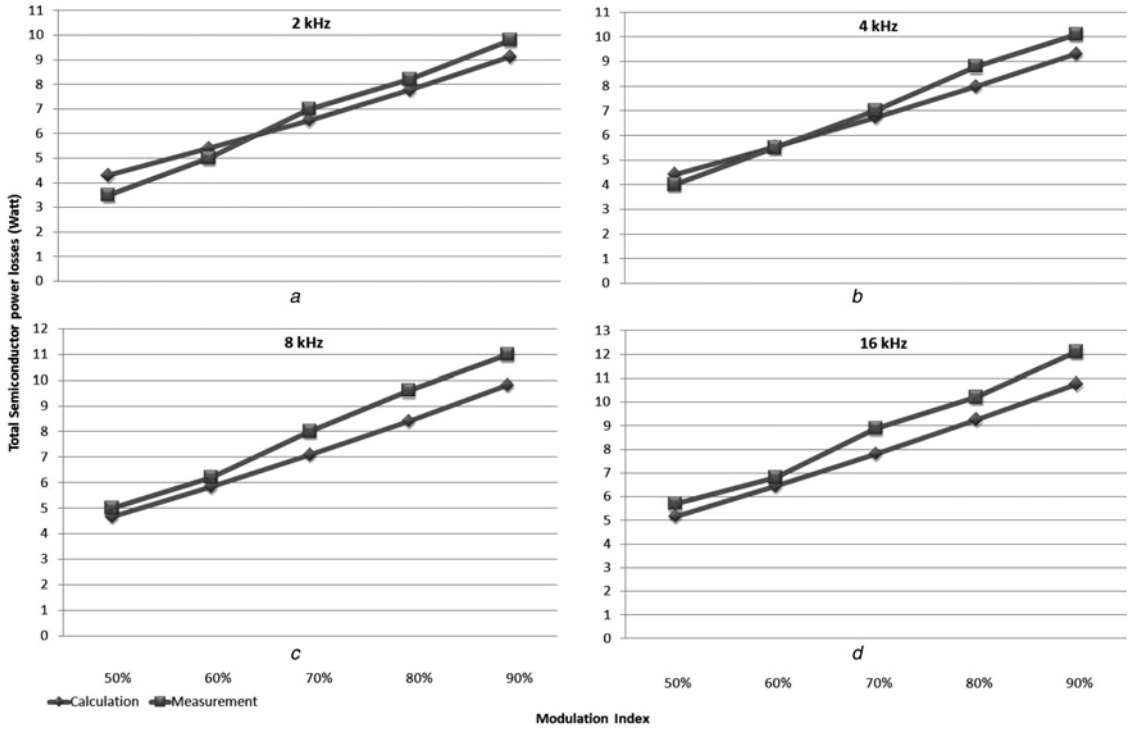

Fig. 10 *Comparing simulated total semiconductor power losses (including switching and conduction losses) with those of practical measurement when carrier frequency*

a 2 kHz
b 4 kHz
c 8 kHz
d 16 kHz

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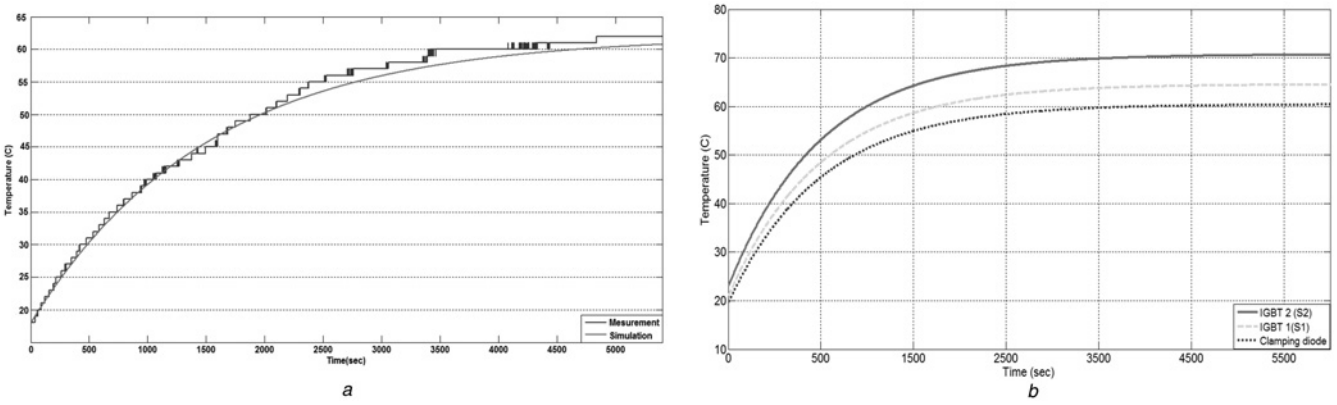

Fig. 11 *Comparison of simulated and measured temperature rise*

a Comparing simulated temperature rise of heatsink with those of the experimental measurement
b Simulated junction temperature rise for the IGBTs (including freewheeling diode) as well as the clamping diode when switching frequency is 1 kHz

evident that practical and theoretical outcomes are very close except for low modulation index that energy relates to the current nonlinearly. This also shows the validity of the modelling of inverter as well as the method of loss calculation. In the mean time, power loss data can be used for calculation of other topics such as designing the size of inverter, selecting the switches and proper heatsink along with cooling systems.

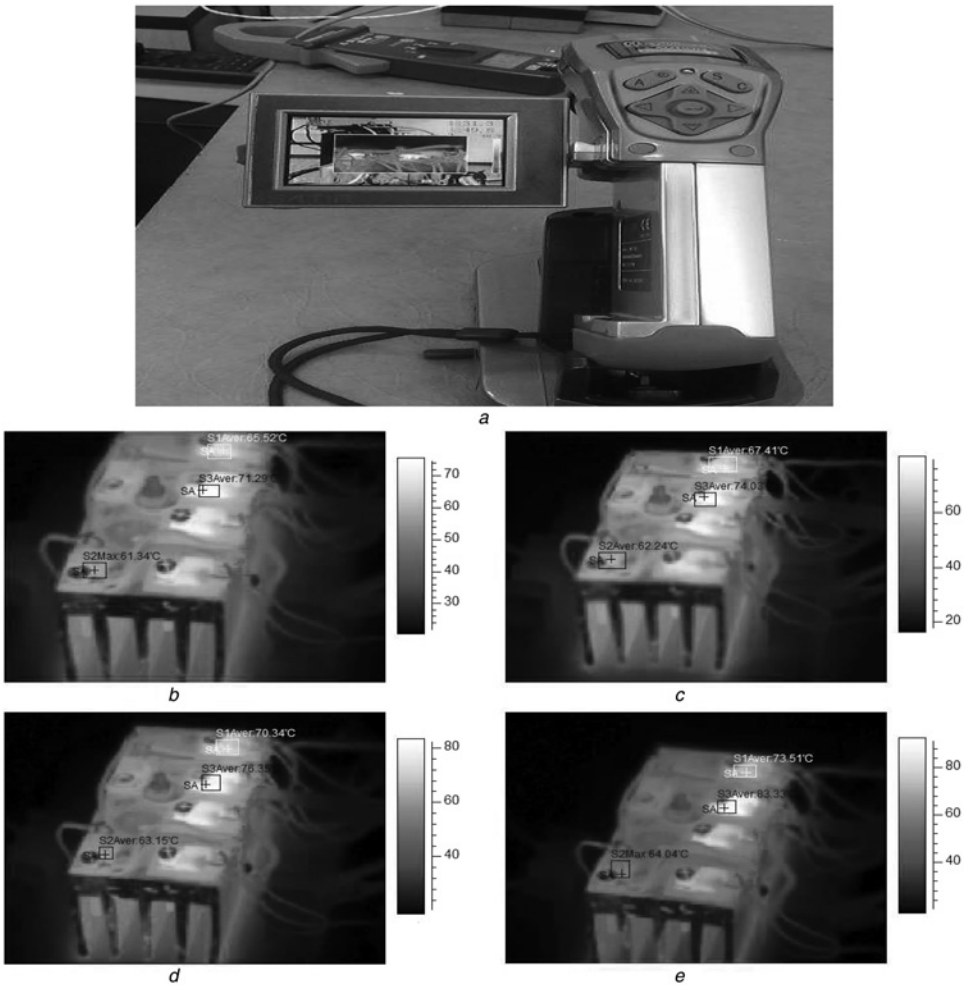

Fig. 12 *Thermography of one leg of the three-level inverter when temperature reaches its final value at switching frequencies*

a The employed thermo-vision camera
b 2 kHz
c 4 kHz
d 8 kHz
e 16 kHz

Table 2 Comparing the final temperatures of both simulations and measurements for two IGBTs (including freewheeling diode) and one diode

	Calculated temperatures, °C				Measured temperatures, °C			
Switching frequency	2 kHz	4 kHz	8 kHz	16 kHz	2 kHz	4 kHz	8 kHz	16 kHz
IGBT 1 (S_1)	64.47	65.11	67	70.44	65.52	67.41	70.34	73.51
IGBT 2 (S_2)	70.9	71.49	74.96	81.51	71.29	74.03	76.35	83.33
clamping diode	60.29	61	62.84	66.31	61.34	62.24	63.15	64.04

In brief, the practical results show that the developed software is quite accurate and reliable. Hence, simulated transient curves for power losses could be used in predicting the lifetime of semiconductors because the key curve for lifetime estimation is transient thermal curve. It should be emphasized that generation of these thermal curves, especially under high frequencies, could not be accurately measured in laboratories because of considerable time delay in thermal sensors.

6.2 Thermography of the three-level inverter

In this step, a digital multimeter connected to the PC (Fig. 8) for recording the heatsink temperature rise using a thermocouple. This experimental set up can validates the result of heatsink thermal simulation that is shown in Fig. 3*b*.

It takes a long time for the heatsink to reach its final temperature because of its large thermal time constant. In this case, the experiment was continued up to 5400 s until the temperature of heatsink remained constant at 61°C. The comparison of simulated and measured temperature rise is indicated in Fig. 11*a*, showing pretty accurate match. The ambient temperature (T_{Amb}) is 22°C, and the heatsink to ambient temperature rise (ΔT_{HA}) is 39°C according to the experiment.

Fig. 11*b* shows simulated variations in the junction temperature of semiconductors up to 5500 s when switching frequency is 2 kHz. To validate simulations, a measuring device is needed, that is capable of measuring junction temperature. The usual thermometers have no access to the junction, just measuring the case temperature. Therefore a thermo-vision camera (see Fig. 12*a*) was used to measure junction temperature of semiconductors.

An experiment was arranged in which the load is the same as the performed simulations for semiconductors. Also, the modulation index and switching frequency are 90% and 2 kHz, respectively. Fig. 12*b* shows thermography of one phase of inverter for 5400 s. The final temperature of each component is indicated on the picture. It can be seen from Fig. 12*b* that the central IGBTs (S_2, S_3) are hotter than (S_1, S_4) because of their higher power losses. This issue has also been indicated in simulations shown in Fig. 11*b*. Figs. 12*c* and *d* demonstrates similar experiment when the switching frequency is increased to 4, 8 and 16 kHz. Table 2 summarises final temperatures related to semiconductors of one leg of the three-level inverter, both for simulations and experiments at 2, 4, 8 and 16 kHz.

7 Conclusion

Multilevel converters are gaining their position in industrial applications. Hence, it is essential to have a precise evaluation from their efficiency and performance in practice. At the same time, generation of thermal curves for semiconductor switches could become critical when switching frequency gets higher. This paper presents an accurate model for conduction and switching power losses at any given switching frequency and modulation index. This model and procedure were programmed in order to achieve real-time calculation and simulation. Moreover, dynamic thermal model of IGBT and diodes were added to the developed software by applying the instant power losses to thermal transfer functions as input. Thus, the program can accomplish heating curves of semiconductors, even under high switching frequencies. Further, the extracted data from the transient heating curves of components can be used to analyse the number of power cycles that increases the likelihood to failure, a measuring tool as lifetime prediction. All mentioned models and procedures have been collected to a unit software and just with running only one program all results will be available. To verify the developed software, a test setup was arranged in which a three-level diode clamped inverter supplies the load. A DSP controller (TMS320F2834) manages the required pulses for 12 IGBTs of the inverter, where auxiliary devices are provided such as monitoring and driving circuits as well as heatsinks. Comparing experimental results with those of simulated program confirms the developed models and software. Therefore the suggested model along with the developed software can be used as a replacement for related measuring devices.

In the future work, two- and three-dimensional thermal analysis of different types of semiconductors will be investigated and based on accurate electrical and thermal models, a comprehensive aging model for semiconductors is proposed.

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