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Published in IET Power Electronics
Received on 30th November 2013
Revised on 15th June 2014
Accepted on 18th July 2014
doi: 10.1049/iet-pel.2013.0872

ISSN 1755-4535



# Classification of multilevel converters with a modular reduced structure: implementing a prominent 31-level 5 kVA class B converter

*Mohammad Jafar Mojibian, Mohammad Tavakoli Bina*

*Electrical Faculty, K. N. Toosi University of Technology, P.O. Box 16315-1355, Tehran, Iran*
*E-mail: mojibian@ee.kntu.ac.ir*

**Abstract:** Multilevel converters are capable of generating AC voltages with low-total harmonic distortion, applicable to power system applications such as penetration of renewable sources in an active network. These types of topologies may require large number of switches and power supplies, having complex structures along with complicated control algorithms. Recently, a branch of multilevel converters is emerged, in which their 'reduced structure' topologies use lower number of devices compared to the available topologies. This study concentrates on classification of the branched 'multilevel converters' with a 'reduced structure' (MCRS) that lowers the number of semiconductor switches as well as their gate-drivers. Then, these classified structures are compared in terms of their number of power supplies and switches, the number of gate-drivers, breaking voltages of the switches and so on. This will pave the way for the introduction of a structure named B2 in the defined class B among the available MCRS topologies with the lowest number of power electronic devices; this structure is obtained by modifying the structure A2 in the defined class A. Moreover, design and simulation of a 31-level converter is analysed under optimal number of DC sources for all named structures. A laboratory prototype was implemented that verifies operation and performance of the suggested structure B2.

## 1 Introduction

Multilevel converters have been growing in various industrial high-power medium-voltage applications; several topologies can be found in the literature (e.g. [1–5]) in order to overcome the limited semiconductor voltage and current ratings. One advantage of such converters is their ability to synthesise waveforms with higher voltage levels, introducing a solution to increase the converter operating voltage above the voltage limits of classical semiconductors [6]. Another significant advantage of multilevel configurations is their capacity in harmonic reduction, without increasing switching frequency nor decreasing the converter output power [7, 8]. Other advantages are the smaller filter size, low $dV/dt$ and reduction in electromagnetic interference. The multilevel voltage source inverters have been recently applied to many medium or high-power industrial applications such as AC power supplies, renewable energies, grid-connected devices, high-speed drive systems and high-voltage direct current [8–11]. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources such as photovoltaic (PV), wind and fuel cells that are connected to grid through a multilevel converter for a high-power application [1].

Compared with conventional 2-level converters, major disadvantages of multilevel structures are their high number of power devices, complex circuits and consequently involving in complicated control strategies. These cause increase of cost, reduction in reliability, complexity in fault detection and maintenance of the converter. In practice, it would be critical to lower the number of switches, gate drives and DC sources used in the converter. This paper considers the most recent 'multilevel converters' with a 'reduced structure' (MCRS) in which the MCRS can be defined as 'a family of multilevel converters in which the number of switches, DC sources or gate-driver circuits are reduced in comparison with those of the conventional multilevel converters for a given number of levels'. Alternatively, if the number of switches is the same both for the MCRS and the conventional multilevel converters, then the number of generated levels is higher for that of the MCRS. As an example, one can compare symmetrical cascaded H-bridge (CHB) converters with those of the asymmetrical ones. Hence, this paper classifies the MCRS based on their inherent specifications into classes A and B in order to get a broader insight into the MCRS. Then, they are compared with each other using an analytical description of each structure in terms of different parameters against the number of levels. These parameters are the number of switches, gate drivers, blocking voltages of the switches and so on, subjected to the optimal number of DC sources for each structure.

The conventional topologies are the basis for new researchers to develop a novel MCRS family of multilevel converters with lower number of power electronic devices.

This paper only considers development of those converters that include all kinds of controllable switches. The MCRS family recently has been included in the literature by introducing numerous advantages both in cost and efficiency of the multilevel converters; they were applied as energy conversion and generation like PV [12–14], fuel cell [15], drive [13, 16, 17], power quality [14, 17], special medical or military applications [17] and so on. The industrial trend shows significant interest in lowering the cost of multilevel converters as well.

Note that asymmetrical cascaded topologies are capable of generating more voltage levels compared with those of symmetrical ones. Hence, asymmetrical cascaded structures are located in the MCRS family compared with those of symmetrical cascaded topologies. Therefore, all studied structures in this paper are of asymmetrical type in order to perform a comprehensive comparison among the introduced MCRS. These detailed comparisons will lead to structure B2 that shows the best performance in terms of the stated parameters among all the introduced structures within the two classes. This selected converter is fully analysed, designed and simulated for a 31-level converter. The designed 31-level class B2 converter was implemented for a 5 kVA power rating. Experiments verify the analysis and simulations of the designed reduced structure.

## 2 Classification of the MCRS

Here, the MCRS are classified in order to discuss them on their overall characteristics instead of looking at them as disparate items. This enables researchers in the field to simply understand the characteristics and specifications involved in the proposed topologies; it would be easier to bridge different topologies in order to fill possible practical notches. Thus, different reduced structure topologies are studied that have appeared in recent years. Surveying lectures on multilevel converters showed us that the MCRS family includes two distinctive categories; the first category allows each DC source appears at the output independently for each stage and the second category provides sequentially added DC voltages at the output for each stage. Regulation of DC capacitor voltages (charge/discharge) is easier for the first category compared with the second one. These facts made us to think of two different classes; some structures fall within the first class, and some others within the second one. Hence, authors suggested classes A and B for the two stated categories. In the meantime, this can be extended in the future just in case a novel class will appear in the literature. The following subsection describes these two categories for the reduced structure multilevel converters that are based on their DC voltage sources.

### 2.1 MCRS: class A

Different topologies can be found in this class, where the available DC sources of the modules (stages) appear independently at their outputs. This principal common characteristic allows appearance of various examples, introducing topologies emerged in the literature. One example could be the family of CHB converters, which under certain conditions falls within the MCRS family:

(1) *Example 1: structure A1:* Assume the CHB in Fig. 1*a*, where the DC sources could appear at the output either symmetrical or asymmetrical independently; but, by using

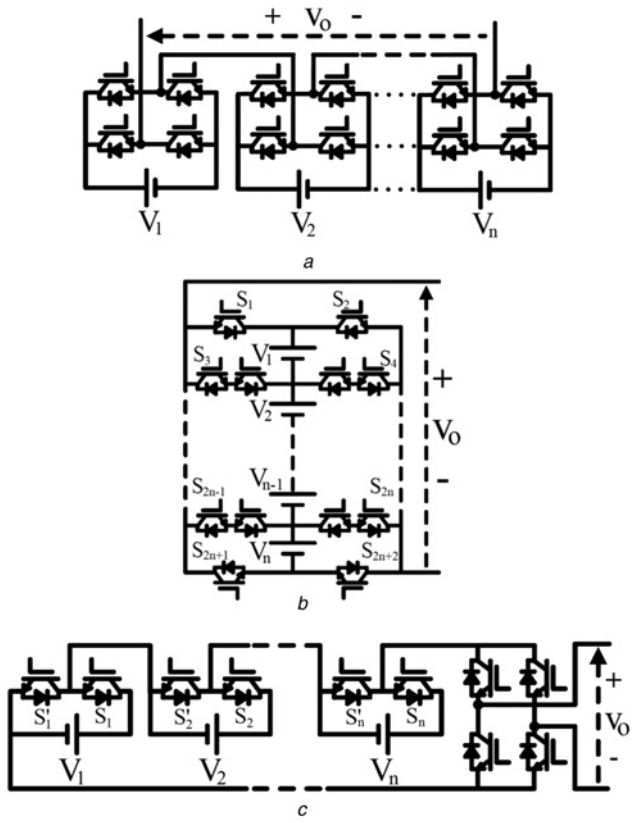


**Fig. 1** *Typical MCRS examples*

*a* Structure A1 example: asymmetrical CHB converter
*b* Structure A2 example: basic extended CHB converter
*c* Structure A3 example: basic cascaded half-bridge converter that is applied to an H-bridge to generate AC voltage

the identical number of CHB, asymmetrical DC sources are capable of producing higher number of levels compared to those of symmetrical sources. For example, 'two symmetrical' CHB generate a 5-level converter; whereas 'two asymmetrical' CHB create a 7-level for the binary [18] (DC voltages are $V_{dc}$, $2V_{dc}$, $4V_{dc}$ etc.) and a 9-level for the trinary [19] (DC voltages are $V_{dc}$, $3V_{dc}$, $9V_{dc}$ etc.). This later introduces the 'regeneration' process in the modules with lower powers because of the circulating current between the modules [8]. Hence, asymmetrical CHB falls within the MCRS class A.

(2) *Example 2: structure A2:* The MCRS structure A2 is made up of basic extended CHB that can be cascaded for connecting to high voltage applications. Fig. 1*b* shows one basic extended CHB that is capable of generating positive, zero and negative voltage levels [20]. Each basic module has $n$ DC sources that could emerge independently. Four switches $S_1$, $S_2$, $S_{2n+1}$ and $S_{2n+2}$ are of single-quadrant type. Other remaining switches within each module have to be of bi-directional one, where common-emitter type is more popular because of requiring only one gate-driver per bi-directional switch. Structure A2 creates three output voltage levels per module when each module uses only one DC source; this increases to five levels with two equal DC sources, and seven levels when two DC sources are arranged like the binary ratios. If the number of DC sources increases beyond two, then even the binary ratios cannot be applied.

(3) *Example 3: structure A3:* This structure is made up of cascaded half-bridge (two-level choppers) converters that

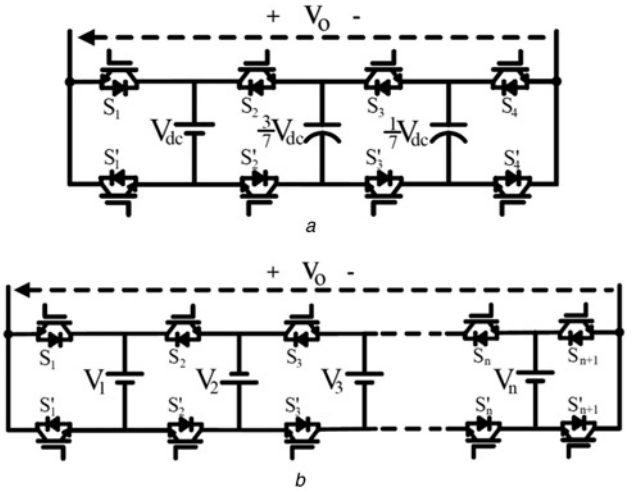


**Fig. 2** *Typical MCRS structure A4 example*

*a* 15-level packed U-cells topology
*b* Extended general structure A4

are capable of generating positive and zero voltage levels. The conventional modular multilevel converter (MMC) utilises two such branches in order to create AC voltage [21]. In [22], one branch of cascaded half-bridge is applied to an H-bridge for generating AC voltage as shown in Fig. 1*c*. Structure A3 is fallen within the MCRS class A because of the lower number of switches involved in operating like that of the MMC. This MCRS class A converter uses high-stress switches for the output H-bridge. The basic cascaded half-bridge in Fig. 1*c* can be further cascaded for creating higher voltage levels.

(4) *Example 4: structure A4:* A packed U-cell multilevel converter topology is introduced in [13] that is composed of one DC source and a number of flying capacitors. This structure has the class A main characteristic, where the DC source is surrounded by four switches and each flying capacitor by two switches. A typical 15-level configuration for such structure is shown in Fig. 2*a*, including one DC source, two capacitors and eight switches.

Structure A4 is basically similar to a reduced structure A1 with a binary voltage ratio arrangement; the difference although is that regeneration has no effect on the binary, whereas it may appear on structure A4. Voltage ratios of the DC sources obey 1, 2 and 4 for the binary, and 1, 3 and 7 for the packed U-cell topology.

One proposition for improving structure A4 is demonstrated in Fig. 2*b*, in which the polarities of DC sources in Fig. 2*a* are changed. Thus, the proposed structure would be capable of removing the regeneration effect as well as providing a modular structure. Note that the DC sources have to be identical in such a module.

## 2.2 MCRS: class B

Unlike class A, the principal characteristic of class B converters is their inability to merge DC sources independently at the output. Instead, the output voltage is sequential summation of DC sources for every switching state. The DC sources have to be identical in order to produce a voltage proportional to the desired output voltage. The MCRS class B family can be introduced by two different topologies.

(1) *Example 1: structure B1:* A basic module for the MCRS structure B1 is shown in Fig. 3*a* in which $n$ DC sources appear at the output sequentially as below [23]

$$V_{\mathrm{O}} = \sum_{k=1}^{m} V_k, \quad m = 1, 2, \ldots, n \tag{1}$$

All switches have to be bi-directional except the first and the last ones. All DC sources are identical, inherently creating non-negative voltage levels that are applied to an H-bridge in order to generate AC voltage as demonstrated in Fig. 3*b* [24]. While the voltage stress on the output H-bridge is high, the basic structure can be cascaded for higher voltages with increased number of levels [23, 24].

Structure B1 also appears in other forms and configurations [12, 25]. Furthermore, the modules of this structure is introduced in [26] by using unidirectional switches; while the number of switches is the same as other structures, but the number of gate-driver circuits is increased because of the lack of bi-directional switches.

(2) *Example 2: suggestion of structure B2:* Consider structure A2 that is schematically shown in Fig. 3*c*. This structure is capable of appearing in the DC sources at the output

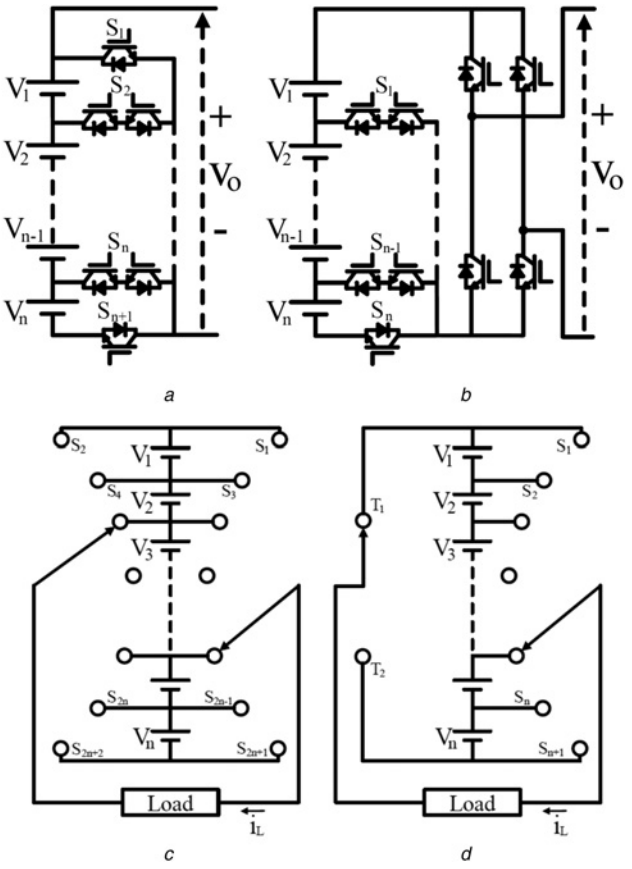


**Fig. 3** *Typical MCRS structure examples with bi-directional switches*

*a* Basic fundamental module of structure B2 example with sequential DC sources
*b* Connection of an H-bridge at the output of the basic module to generate AC voltage
*c* General diagram of the MCRS structure A2 with bi-directional switches
*d* Suggested general diagram of the MCRS structure B2 by removing bi-directional switches from the left-hand side of Fig. 3*c*




doi: 10.1049/iet-pel.2013.0872

independently. Now let us suggest the removal of the left-hand side bi-directional switches, maintaining only two single-quarter switches as shown in Fig. 3*d*.

Unlike the basic module of structure A2, the suggested MCRS structure B2 is capable of producing positive, zero and negative levels within the interval $-nV_{dc}$, $-(n-1)V_{dc}$, …, $-V_{dc}$, 0, $V_{dc}$, $2V_{dc}$, …, $nV_{dc}$. The advantage of producing negative levels in addition to the positive and zero levels is coined with a change from classes A to B; this implies the independent appearance of DC sources are converted to a sequential appearance. This paper concentrates on the MCRS suggested structure B2, examining its characteristics and operation in detail using the implemented laboratory prototype. It should also be noted that, unlike structure A2, every voltage level is related to a single-switching state for structure B2. Hence, structure B2 is capable of producing the same number of voltage levels as structure A2; but, with the lower number of switches.

## 3 Theoretical description of the MCRS classes

This section compares all MCRS structures introduced in classes A and B analytically in order to obtain the number of DC sources, the number of switches, the number of output voltage levels, stresses on the switches and so on. Since the concentration of this research is structure B2, here the mathematical description of this structure is detailed typically; the other structures in both classes are then extracted similarly (not detailed here) and summarised in Table 1.

Assume Fig. 4 in which $m$ cascaded structure B2 is presented; also, the number of identical DC sources within $m$ basic modules are $n_1$, $n_2$, …, $n_m$. Let us further assume $n_1$ DC sources from the first module are all equal to $V_{dc}$. Then, the first module is capable of generating $2n_1+1$ output voltage levels. To avoid the regeneration phenomenon along with obtaining the most possible number of levels, all DC sources within the second module

**Table 1** Parameters calculated for different structures in both classes for a fixed $N_{level}$ based on optimised number of DC sources

| Parameter | Structures in class A | | | | Structures in class B | |
|---|---|---|---|---|---|---|
| | A1 (binary) | A2 | A3 | A4 | B1 | B2 |
| $n$ (minimised $N_{switch}$ subjected to a fixed $N_{level}$) | 1 | 1 | 3 | 2 | 2 | 2 |
| $N_{switch}$ | $\frac{4\ln((N_{level}+1)/2)}{\ln(2)}$ | $\frac{8\ln((N_{level}+1)/2)}{\ln(3)}$ | $\frac{10\ln((N_{level}+1)/2)}{\ln(4)}$ | $\frac{6\ln((N_{level}+1)/2)}{\ln(3)}$ | $\frac{7\ln((N_{level}+1)/2)}{\ln(3)}$ | $\frac{6\ln((N_{level}+1)/2)}{\ln(3)}$ |
| $N_{GD}$ | $\frac{4\ln((N_{level}+1)/2)}{\ln(2)}$ | $\frac{6\ln((N_{level}+1)/2)}{\ln(3)}$ | $\frac{10\ln((N_{level}+1)/2)}{\ln(4)}$ | $\frac{6\ln((N_{level}+1)/2)}{\ln(3)}$ | $\frac{6\ln((N_{level}+1)/2)}{\ln(3)}$ | $\frac{5\ln((N_{level}+1)/2)}{\ln(3)}$ |
| $N_{DC}$ | $m$ | $m$ | $3m$ | $2m$ | $2m$ | $2m$ |
| $N_{level}$ | $2^{m+1}-1$ | $2^{m+1}-1$ | $2^{2m+1}-1$ | $2\times3^m-1$ | $2\times3^m-1$ | $2^{m+1}-1$ |
| $V_m$ | $2^{m-1}\times V_{dc}$ | $2^{m-1}\times V_{dc}$ | $4^{m-1}\times V_{dc}$ | $3^{m-1}\times V_{dc}$ | $3^{m-1}\times V_{dc}$ | $2^{m-1}\times V_{dc}$ |
| $V_{SW}/V_{dc}$ | $2(N_{level}-1)$ | $(5/2)(N_{level}-1)$ | $3(N_{level}-1)$ | $2(N_{level}-1)$ | $(11/4)(N_{level}-1)$ | $(9/4)(N_{level}-1)$ |
| $\sigma/V_{dc}$ | $(1/4)(N_{level}-1)$ | $(1/3)(N_{level}-1)$ | $(3/8)(N_{level}-1)$ | $(1/3)(N_{level}-1)$ | $(1/3)(N_{level}-1)$ | $(1/3)(N_{level}-1)$ |

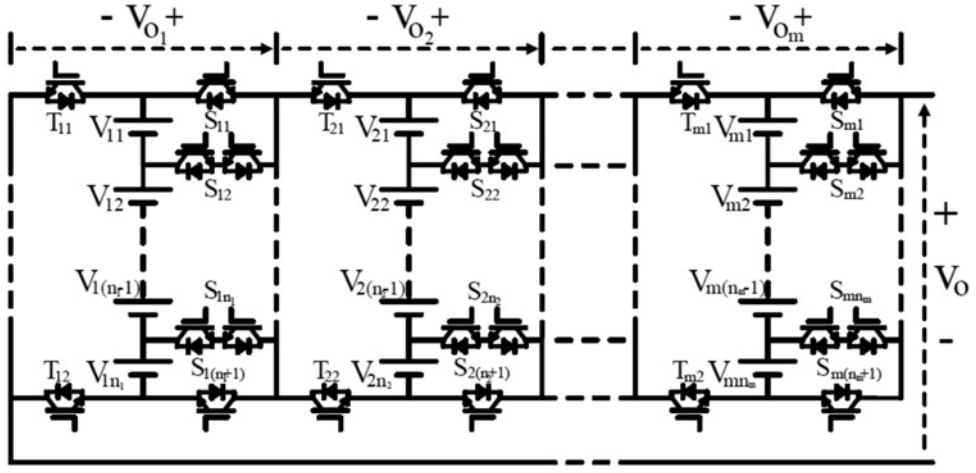


**Fig. 4** *Cascaded topology of structure B2 for mathematical description on voltage levels, number of switches, voltage stresses on switches and so on*

can be selected as below

$$V_{2i} = V_{1i} + \sum_{k=1}^{n_1} V_{1k} = (n_1 + 1)V_{\mathrm{dc}}, \quad i = 1, 2, \ldots, n_2 \quad (2)$$

Hence, the second module is asymmetrical with respect to the first one. Therefore, this can be generalised for further modules to obtain a general description for all DC sources within the $m$th module ($m \geq 2$) as follows

$$\begin{aligned} V_{mi} &= V_{1i} + \sum_{k=1}^{n_1} V_{1k} + \sum_{k=1}^{n_2} V_{1k} + \cdots + \sum_{k=1}^{n_{m-1}} V_{1k} \\ &= \sum_{k=1}^{m-1} \sum_{l=1}^{n_k} V_{kl} = \prod_{k=1}^{m-1} (n_k + 1)V_{\mathrm{dc}}, \quad i = 1, 2, \ldots, n_m \end{aligned} \quad (3)$$

Thus, using the suggested DC sources in (2) and (3), the maximum conceivable output voltage $V_{\mathrm{peak}}$ and the total number of achievable levels $N_{\mathrm{level}}$ are

$$\begin{cases} V_{\mathrm{peak}} = n_1 \times V_{1i} + n_2 \times V_{2i} + \cdots + n_m \times V_{mi} = \sum_{k=1}^{m} (n_k \times V_{ki}) \\ N_{\mathrm{level}} = 2\prod_{k=1}^{m} (n_k + 1) - 1 \end{cases} \quad (4)$$

Also, the total number of DC sources $N_{\mathrm{dc}}$ and total number of switches $N_{\mathrm{switch}}$ for $m$ modules are

$$\begin{cases} N_{\mathrm{dc}} = n_1 + n_2 + \cdots + n_m = \sum_{k=1}^{m} n_k \\ N_{\mathrm{switch}} = \sum_{k=1}^{m} [(n_k - 1) \times 2 + 4] = \sum_{k=1}^{m} 2 \times (n_k + 1) \end{cases} \quad (5)$$

Assume it is desired to maximise $N_{\mathrm{level}}$ in (4) subjected to a fixed $N_{\mathrm{dc}}$ or $N_{\mathrm{switch}}$ in (5). Then, $N_{\mathrm{level}}$ is maximised when all terms in the right-hand side of (4) are identical ($n_1 = n_2 = \cdots = n_m = n$). Hence, applying this consideration in (5) results in

$$\begin{cases} N_{\mathrm{switch}} = 2m(n + 1) \\ N_{\mathrm{level}} = 2(n + 1)^m - 1 \end{cases} \quad (6)$$

A relationship can be developed between $N_{\mathrm{switch}}$ and $N_{\mathrm{level}}$ by omitting $m$ from the two equations in (6)

$$N_{\mathrm{level}} = 2(n + 1)^{((N_{\mathrm{switch}})/(2(n+1)))} \quad (7)$$

Since each bi-directional switch of common-emitter type needs only one gate-driver, the total number of gate-drivers ($N_{\mathrm{GD}}$) can be given as below

$$N_{\mathrm{GD}} = m\big[(n - 1) + 4\big] = m(n + 3) \quad (8)$$

Combination of (6) with (8) results in a relationship that the number of gate-drivers is given in terms of the number of levels and the number of DC sources of each module

$$N_{\mathrm{GD}} = \frac{\ln\big((N_{\mathrm{level}} + 1)/2\big)}{\ln(n + 1)}(n + 3) \quad (9)$$

The maximum possible voltage stress on the converter switches ($V_{\mathrm{SW}}$) can be worked out with respect to the breaking voltage of unidirectional ($V_{\mathrm{SW,u}}$) and bidirectional ($V_{\mathrm{SW,b}}$) switches as below

$$\begin{cases} V_{\mathrm{SW}} = V_{\mathrm{SW,u}} + V_{\mathrm{SW,b}} = \left(2 + \frac{H}{2n}\right)(N_{\mathrm{level}} - 1)V_{\mathrm{dc}} \\ V_{\mathrm{SW,b}} = H(V_{1i} + V_{2i} + \cdots + V_{mi}) = HV_{\mathrm{dc}}\left(\frac{(n+1)^m - 1}{n}\right) \\ V_{\mathrm{SW,u},k} = 4(V_{k1} + V_{k2} + \cdots + V_{kn}) = 4n(n+1)^{k-1}V_{\mathrm{dc}} \\ V_{\mathrm{SW,u}} = V_{\mathrm{SW,u},1} + V_{\mathrm{SW,u},2} + \cdots + V_{\mathrm{SW,u},m} = ((n+1)^m - 1)V_{\mathrm{dc}} \\ H = \begin{cases} \frac{3n^2}{4} - n & n \text{ is even} \\ \frac{3n^2 + 1}{4} - n & n \text{ is odd} \end{cases} \end{cases} \quad (10)$$

Table 1 shows the above summarised calculated parameters for structure B2; similar analysis was carried out for other explained structures with the optimal number of DC sources in both classes, and listed in Table 1 as well.

## 4 Analytical comparison of the classified MCRS

Looking into the parameters obtained in Table 1, it can be explained similarities and differences of the two classes. The comparisons are based on the optimally designed parameters of different structures in both classes to maximise the number of levels; the number of DC sources in all modules is identical. In the meantime, it is assumed that all structures employ the optimised number of DC sources in each module (see Table 1). Under this circumstance, both structures A2 and A1 would be the same. Thus, it is important to consider two DC sources in each module for structure A2 to avoid elimination of one structure from the comparison. Hence, the following analytical comparisons are studied to select the best configuration.

### 4.1 Number of switches

Fig. 5*a* compares the required number of switches against the maximised number of voltage levels (MNVL) for all structures. It can be seen that the two structures A4 and B2 employ the lowest number of switches whereas the two structures A2 and A3 use the highest.

### 4.2 Number of gate-drivers

The number of gate-drivers is demonstrated in Fig. 5*b* against the MNVL. It is evident that structure B2 needs the least number of gate-drivers compared with those of other structures.



*IET Power Electron.*, 2015, Vol. 8, Iss. 1, pp. 20–32
doi: 10.1049/iet-pel.2013.0872

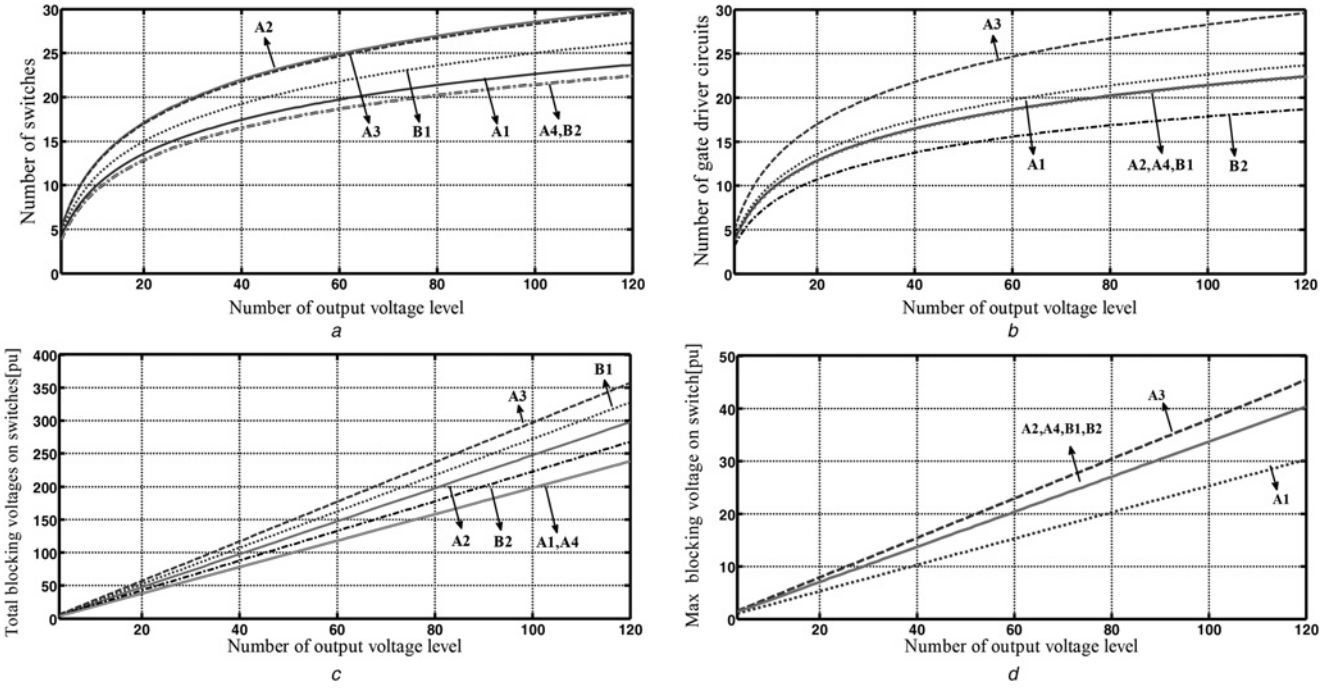


**Fig. 5** *Required number of*

*a* Switches
*b* Gate-drivers for all structures against $N_{level}$
The normalised breaking voltage of the switches based on $V_{dc}$ for all structures against $N_{level}$
*c* Total breaking voltage
*d* Maximum breaking voltage

### 4.3 Breaking voltages of the switches

Fig. 5*c* depicts the total breaking voltages of all switches for each structure ($V_{SW}$) against $N_{level}$. This summated voltage is normalised by $V_{dc}$. The total breaking voltage $V_{SW}$ can be characterised as a typical rating for the converter switches as well as the switching losses of the converter. Analytical studies show that structures A1 and A4 have the lowest $V_{SW}$, and structure B2 locates on the second place. In the meantime, Fig. 5*d* shows that the maximum breaking voltage ($\sigma$) within structure A1 is the smallest, whereas this is the biggest for structure A3.

### 4.4 Selection of the best structure

Comparing various structures in both classes show the following realities according to the foregoing discussions:

- The suggested reduced structure B2 is the optimal one among all structures in terms of the lowest number of both switches and gate-driver circuits (see Figs. 5*a* and *b*).
- Two reduced structures A1 and A4 are the optimal ones in terms of the lowest total breaking voltage and the maximum breaking voltage (see Figs. 5*c* and *d*).

Considering the above facts, one can select the best configuration based on the required applications as below:

- Assuming a given number of switches, the reduced structures A1 and A4 can be utilised for medium and high voltage applications since the breaking voltages for such topology is the lowest among other structures.
- Assuming a given number of levels, the reduced structure B2 can be utilised for applications that employ converters with more elements in a cascaded configuration. In other words, assume a given application is employed, a conventional converter that needs a certain number of power electronic devices such as switches, DC sources and gate driver circuits. The same application can be implemented with the reduced structure B2 in which the stated power electronic devices are lower than the conventional one, even lower than the other named structures.

This research will be continued by design and implementation of structure B2 to confirm its capabilities for the discussed analysis and simulations.

### 4.5 Comparing the MCRS with their related standard topologies

Let us compare the introduced MCRS topologies with their related basic structures in order to have a broader outlook to the general achievements of the new topologies. This comparison is conducted based on designing a 31-level two-stage converter. Hence, Table 2 is arranged such that the first five columns are dedicated to the MCRS in comparison with the second four columns that is related to the conventional standard topologies. It can be seen from Table 2 that, for building up a 31-level converter, standard topologies need bigger numbers of power electronic devices compared to the six named structures in both classes of the MCRS. Table 2 also explains which standard conventional topology of multilevel converters is developed to obtain each of the six structures in the MCRS. For example, structure A1 is obtained from the standard symmetrical CHB converter.

**Table 2** Comparing design parameters for all the classified MCRS structures with those of standard multilevel topologies

| MCRS | | | | | Related standard topology | | | |
|---|---|---|---|---|---|---|---|---|
| Class | Structure | 31-level asymmetric converter ($m=2$) | | | Basic structure | 31-level symmetric converter ($m=2$) | | |
| | | $N_{switch}$ | $N_{GD}$ | $N_{DC}$ | | $N_{switch}$ | $N_{GD}$ | $N_{DC}$ |
| A | A1 | 16 | 16 | 4 | symmetric CHB | 60 | 60 | 15 |
| | A2 | 24 | 16 | 6 | extended HB | 60 | 34 | 15 |
| | A3 | 20 | 20 | 6 | cascaded half bridge (MMC) | 60 | 60 | 30 |
| | A4 | 16 | 16 | 6 | packed U-cell (FC-CHB) | 34 | 34 | 15 |
| B | B1 | 20 | 16 | 6 | extended half bridge | 38 | 25 | 15 |
| | B2 | 16 | 12 | 6 | extended HB (A2) | 34 | 21 | 15 |

## 5 Design of structure B2

### 5.1 Power circuit design

Assuming a given number of levels, here it is explained the design of a single-phase converter with the reduced structure B2. Assume $N_{level} \geq 30$ is desired, where identical number of two sources is considered per module (optimal design with $n=2$). Thus, the required number of modules ($m$) is equal to 2.5 according to (6). Since $m$ has to be an integer, choosing $m=2$ results in $N_{level}=25$, and $m=3$ gives $N_{level}=53$; both rather far from the assumed region. Then, considering $n=3$ would result in $m=2$ according to (6) with 31 levels that is very close to our assumption. Let us also suppose the rms output voltage is 110 V with a peak voltage 155.6 V.

The above basic assumptions can be applied to (3)–(10) (or using Table 1) in order to get other design parameters for structure B2. Table 3 lists these calculated parameters for two cases; $m=2$ and $n=3$. It can be seen from Table 3 that the closest configuration to 30 levels would be two cascaded modules, where each module consists of three identical DC sources. Fig. 6 shows two possible combinations for such a selected set of parameters for structure B2. Either can be chosen for implementation, where the configuration in Fig. 6*b* was implemented because of easy wiring.

Identical DC source voltages can be worked out using

$$v_{o-\max} = 156\,\text{V} = \left((n+1)^m - 1\right)V_{dc} \tag{11}$$

where substituting $m=2$ and $n=3$ in (11) results in $V_{dc}=10.5$ V. Then, all DC source voltages in the first module are equal to 10.5 V, while DC sources in the second module are obtained 42.0 V according to (2). The total breaking voltage for unidirectional switches is 630 V, and it is 210 V for bi-directional switches according to (10). Also, the maximum voltage stress, equivalent to 126 V, drops on unidirectional switches of the second module. To have a clear picture on the classified structures for the MCRS, Table 4 provides design parameters for all six structures. In general, structure B2 introduces lower numbers of gate-drivers as well as lower number of switches as shown in Table 4. This structure also demonstrates the highest total points compared with other structures.

**Table 3** Calculated design parameters for the MCRS structure B2 for various number of modules and identical DC sources

| $n$ | $m$ | $N_{level}$ | $N_{switch}$ | $N_{GD}$ | $N_{DC}$ | Variety in DC source voltages |
|---|---|---|---|---|---|---|
| 2 | 2 | 25 | 12 | 10 | 4 | 2 |
| | 3 | 53 | 18 | 15 | 6 | 3 |
| 3 | 2 | 31 | 16 | 12 | 6 | 2 |
| | 3 | 127 | 24 | 18 | 9 | 3 |

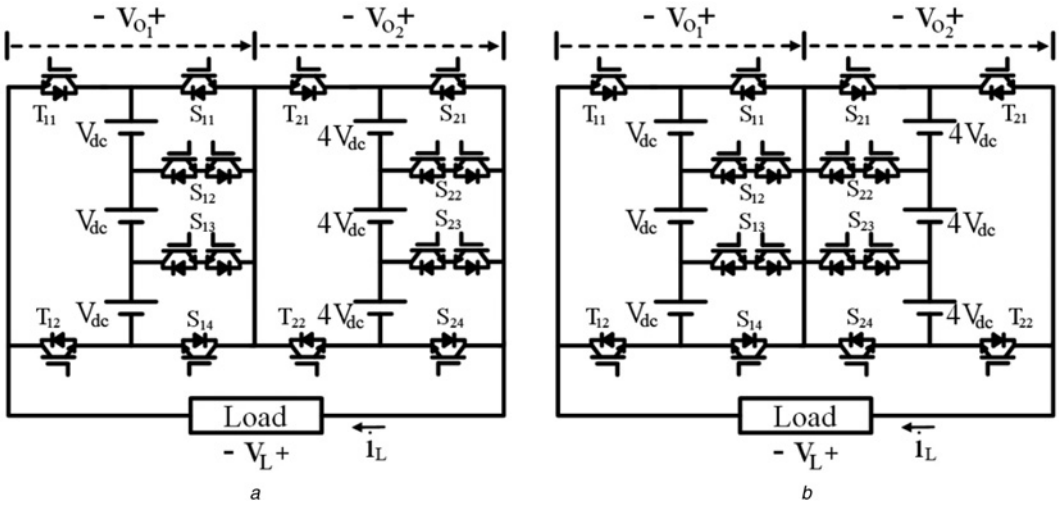


**Fig. 6** *Two possible MCRS structures for B2 (m = 2 and n = 3)*

*a* Normal structure
*b* Easy wiring structure




doi: 10.1049/iet-pel.2013.0872

**Table 4** Comparing design parameters for all the classified MCRS structures

| | $n$ | $m$ | $N_{switch}$ | $N_{GD}$ | $N_{DC}$ | $V_{SW,\ b}$ | $V_{SW,\ u}$ | $\sigma$ | Variety in DC source voltages |
|---|---|---|---|---|---|---|---|---|---|
| A1 | 1 | 4 | 16 | 16 | 4 | – | 630 | 84 | 4 |
| A2 | 3 | 2 | 24 | 16 | 6 | 420 | 630 | 126 | 2 |
| A3 | 3 | 2 | 20 | 20 | 6 | – | 945 | 126 | 2 |
| A4 | 3 | 2 | 16 | 16 | 6 | – | 630 | 84 | 2 |
| B1 | 3 | 2 | 20 | 16 | 6 | 210 | 787.5 | 126 | 2 |
| B2 | 3 | 2 | 16 | 12 | 6 | 210 | 630 | 126 | 2 |

**Table 5** Switching states for structure B2 under fundamental modulation technique

| Switches states | | | | | | | | | | | | $v_o/V_{dc}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Stage1 | | | | | | Stage2 | | | | | | |
| $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | $T_{11}$ | $T_{12}$ | $S_{21}$ | $S_{22}$ | $S_{23}$ | $S_{24}$ | $T_{21}$ | $T_{22}$ | |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 15 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 14 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | −1 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | −14 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | −15 |

### 5.2 Switching states

Different modulation techniques are available for multilevel converters in order to follow a particular goal [27–30]. When the number of levels is high, then the fundamental switching technique could be a useful modulation method [31]. One advantage for this technique is its low switching frequency in comparison with other techniques. Table 5 shows a look-up table for switching states of 31 different levels involved in the designed structure B2 (see Fig. 6*b*). This table shows that only two switches per module are turned on for every state. This is lower than those of other structures, presenting a high efficiency MCRS with low conductive switching losses.

The implemented 31-level structure B2 was modulated with the fundamental technique as shown in Fig. 7 in order to clarify the engaged technique. The 31-level converter is controlled in an open-loop manner by applying a sinusoidal reference for building up the required instantaneous voltage level. In fact, the reference voltage is a 50 Hz sinusoidal voltage having a peak of 315 V that the implemented converter has to generate it in 31 levels. The main objective is to create an output voltage with a slim difference from the desired reference.

## 6 Simulations and experiments

This section starts with the introduction of simulations for the designed structure B2; then, the implemented 5 kVA MCRS structure B2 is presented that verifies the performed analysis and simulations. It is noticeable that the batteries in structure B2 can be supplied by a PV energy source (or fuel cell etc.) in practice. Then, all the average DC voltages of the batteries have to be controlled using a state-of-charge (SOC) controller [14] or a battery management system [32]. In a laboratory this has not been performed since the batteries were controlled by relevant power supplies in order to focus on the performance of structure B2.

### 6.1 Simulations

Structure B2 provides high number of output levels if the number of DC voltage sources is increased; for example, up to 31 levels will be available, only if three DC voltage sources are involved in each module of a two stage converter. Hence, a 31-level structure B2 was simulated according to Fig. 6*b*. The switches of the converter are

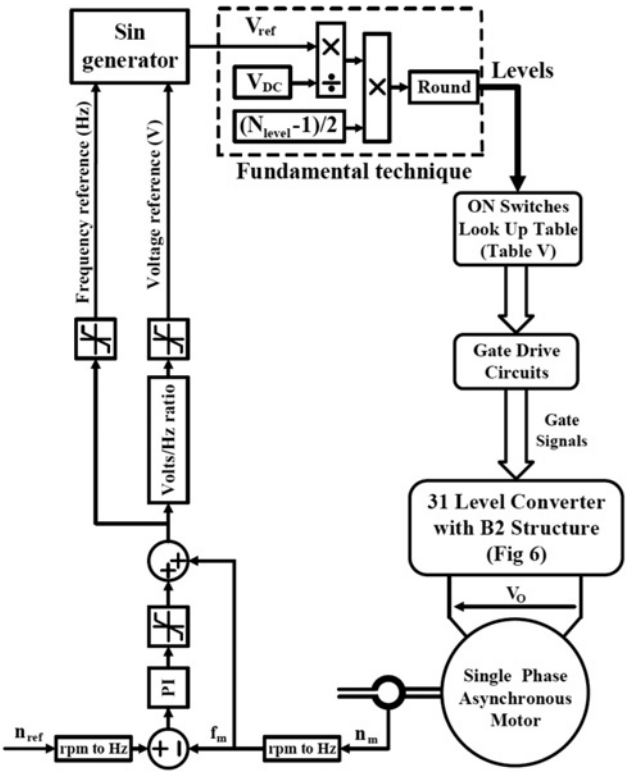


**Fig. 7** *Closed-loop control scheme for adjusting speed drive of a single-phase asynchronous motor using a 31-level converter*

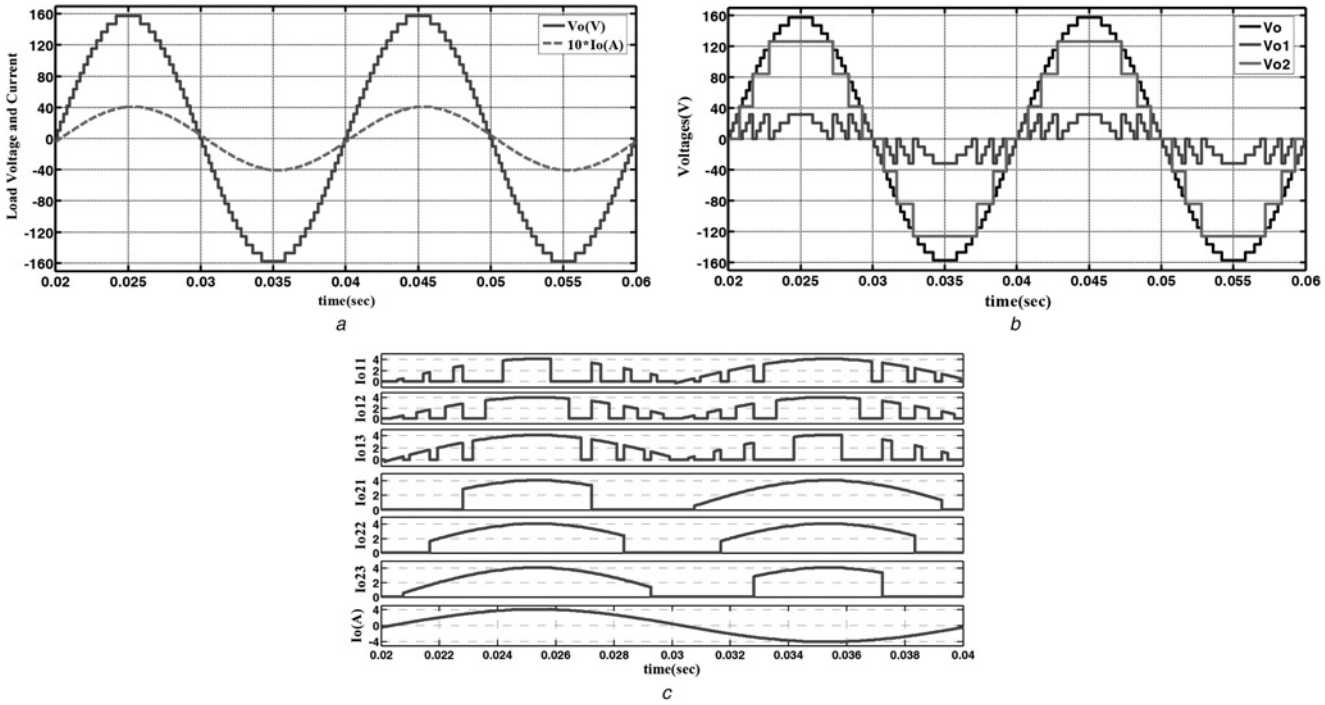


**Fig. 8** *Steady-states simulations*

*a* Simulated output voltage and current of structure B2
*b* Voltages of two modules along with the total voltage
*c* Currents of the DC sources in each module along with the resultant output current

modulated based on the technique discussed in Section 5.2. Structure B2 can be applied to various applications such as renewable energy conversion like PV systems, fuel cell, battery storage and automotive adjustable speed and position control systems. Also, the implemented 31-level topology can be used in single-phase UPS applications that create high-quality sinusoidal AC output. This power converter could be applied to an adjustable speed drive for a single-phase motor.

Simulated output voltage and current of the converter is shown in Fig. 8*a*. The THD of the output voltage and current are 2.62 and 0.50%, respectively, very close to a pure sinusoidal waveform because of the high number of levels. The current (multiplied by ten) is very smooth as shown in Fig. 8*a*. Figs. 8*b* and *c* depict the behaviour of the converter modules, showing the voltage of each module as well as their aggregated voltage in Fig. 8*b*. It can be seen that the switching frequency of the first module is bigger than the other one, contributing to build up the desired output voltage in combination with the second module because of its fast variations. The bigger the number of modules, the lower the switching frequencies of the bottom modules would be. In a medium/high voltage design, one can apply switches with low switching frequencies to the bottom modules (e.g. IGCT), and high switching frequency switches to the upper modules (e.g. IGBT).

Fig. 8*c* illustrates current build up by the DC sources within the two modules. Considering every half cycle, the second DC source in each module is identically repeated, while the waveform of the first DC source is swapped with the third one. This is an advantage for structure B2 that even conventional modulation techniques being naturally capable of identical utilisation of the DC sources in each module. In other words, energy unbalance is prevented for the DC sources in each module. This advantage cannot be seen in

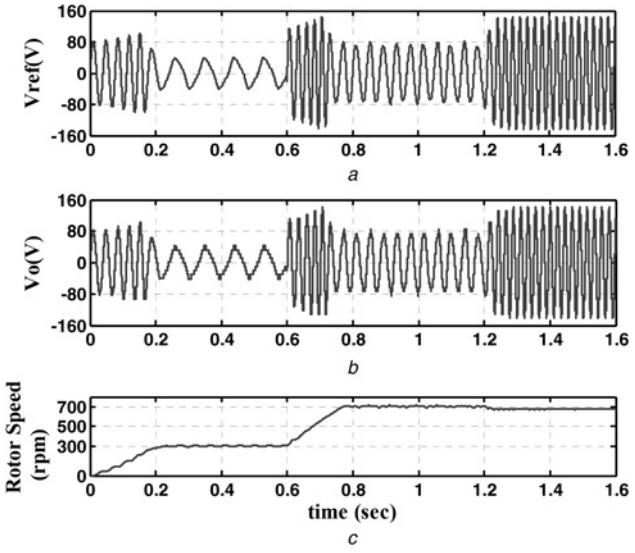


**Fig. 9** *Simulations for the closed-loop control shown in Fig. 7, including the reference voltage, the actual output voltage of the converter and the rotor speed under different working conditions*

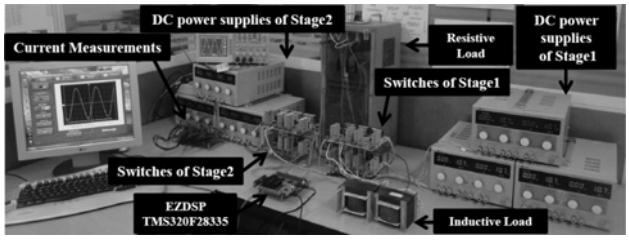


**Fig. 10** *Implemented 5 kVA prototype for structure B2*



*IET Power Electron.*, 2015, Vol. 8, Iss. 1, pp. 20–32
doi: 10.1049/iet-pel.2013.0872

**Table 6** Specifications of the implemented 31-level structure B2

| No | Title | Specifications | Quantity |
|---|---|---|---|
| 1 | IGBT | BUP314, 35 A, 1200 V | 16 |
| 2 | IGBT driver | TLP 250, ±30 V, 1 A | 12 |
| 3 | microprocessor | EZDSP TMS320F28335 | 1 |
| 4 | switching technique | fundamental | – |
| 5 | power supplies stage 1 | 10.5 V | 3 |
| | voltage stage 2 | 42 V | 3 |
| 6 | load | $RL$ ($R$ = 38 Ω, $L$ = 13 mH) | 1 |
| 7 | output voltage (rms) | 110 V | – |
| 8 | load current (rms) | 2.82 A | – |
| 9 | fundamental frequency | 50 Hz | – |

other structures naturally, it may be made possible only by some complex switching techniques. Notice that since the currents of DC sources are non-negative, DC source voltages should be selected correctly. For example, the trinary (structure A1) may encounter the regeneration process if the DC current in the first module becomes negative.

*6.1.1 Control scheme:* Various control schemes were introduced in the literature for multilevel converters [33] that principally are based on determining the desirable instantaneous voltage level for the output. Here, it is also determined the instantaneous voltage level, where the look-up table shown in Table 5 gives those switches that have to be turned on. The implemented 31-level structure B2 was modulated with the fundamental technique as shown in Fig. 7 in order to clarify the engaged technique. The 31-level converter is controlled in an open-loop manner by applying a sinusoidal reference for building up the required instantaneous voltage level.

In the meantime, the simulated could be applied to an adjustable speed drive of a single-phase motor under a closed-loop control design as shown in Fig. 7. This loop is directed towards regulating the required voltage for the motor. The samples of the rotor speed is taken, and then compared with the reference speed. Resultant error makes the reference frequency using a PI-controller. Also, the voltage reference is made using the current status of $v/f$ and the reference frequency. This paves the way for generating the converter sinusoidal reference voltage, where eventually the discussed fundamental modulating procedure applies the needed voltage to the motor. It is noticeable that $V_{DC}$ is the total DC-link voltage of the converter ($V_{DC}$ = 157.5 V).

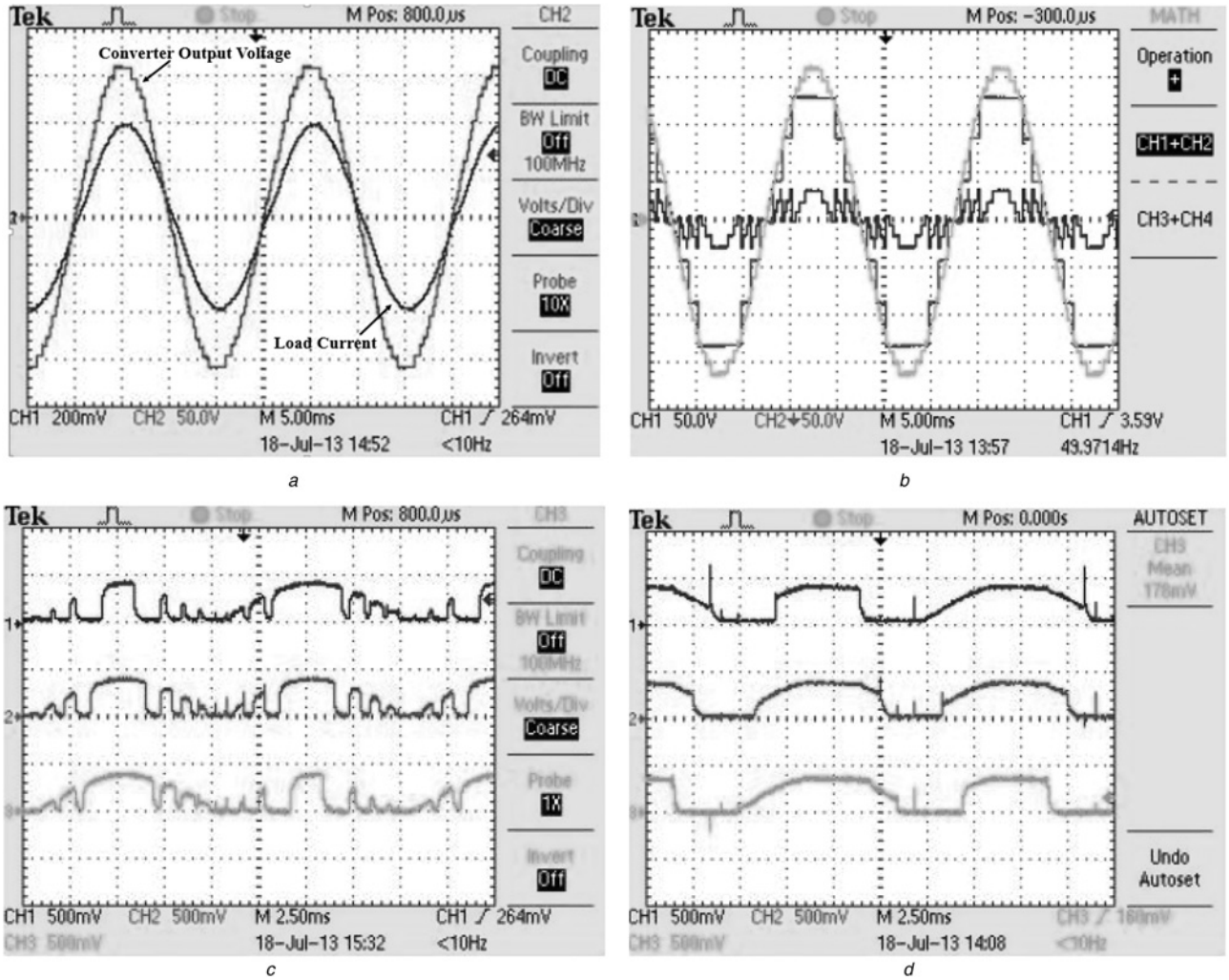


**Fig. 11** *Steady-state operation: experimental performance of structure B2*

*a* Experimental voltage and current of the load (Amp/div = 2 A)
*b* Voltages of two modules along with the total voltage
*c* Currents of the DC sources in module 1
*d* Currents of the DC sources in module 2 (Amp/div = 5 A)

**Table 7** Average currents and powers for the implemented 31-level structure B2

| $P_{11}$ | $P_{12}$ | $P_{13}$ | $P_{21}$ | $P_{22}$ | $P_{23}$ |
|---|---|---|---|---|---|
| 16.6 | 17.6 | 16.6 | 86.9 | 93.2 | 86.9 |
| Average currents and voltages of the DC sources in the two modules | | | | | |
| $I_{11}$, A | $I_{12}$, A | $I_{13}$, A | $I_{21}$, A | $I_{22}$, A | $I_{23}$, A |
| 1.58 | 1.68 | 1.58 | 2.07 | 2.22 | 2.07 |
| $V_{11}$, V | $V_{12}$, V | $V_{13}$, V | $V_{21}$, V | $V_{22}$, V | $V_{23}$, V |
| 10.50 | 10.47 | 10.50 | 41.90 | 41.98 | 41.90 |
| total input power, W | | output power, W | | efficiency, % | |
| 317.8 | | 313.3 | | 98.5 | |

Closed-loop control shown in Fig. 7 were simulated in which speed of an asynchronous motor (110 V, 0.25 hP, 4 poles, 50 Hz) was adjusted. Fig. 9 demonstrates the reference voltage, the converter output as well as the motor speed. First, the motor is started to reach 300 rpm; then, the reference speed is changed to 700 rpm at $t = 0.6$ s. Second, load is changed stepwise by 2 N m at $t = 1.2$ s in order to see the controller behaviour. As can be seen from Fig. 9, the closed-loop easily controls the motor speed at both starting and other operating modes. Also, the control system generates a sinusoidal reference waveform where both frequency and amplitude are variable. Furthermore, the 31-level converter is capable of producing such voltage at its output in order to control both speed and power of the motor.

### 6.2 Experimental validation and analytical discussions

A 5 kVA prototype was implemented to validate the designed MCRS structure B2 (see Section 5) as shown in Fig. 10. The switches are 1200 V, 35 A of IGBT type BUP314. Also, the microprocessor EZDSP TMS320F28335 was used to implement the switching algorithm discussed in Section 5.2. Six isolated low-power DC sources were engaged in supplying the required voltages of each module. Table 6 lists specifications of the designed structure B2.

Fig. 11*a* shows experiments for the load specified in Table 6 including the *RL*-load voltage and current. The THD of voltage and current waveforms are 3.35 and 3.12%, respectively. Comparing experiments with those of

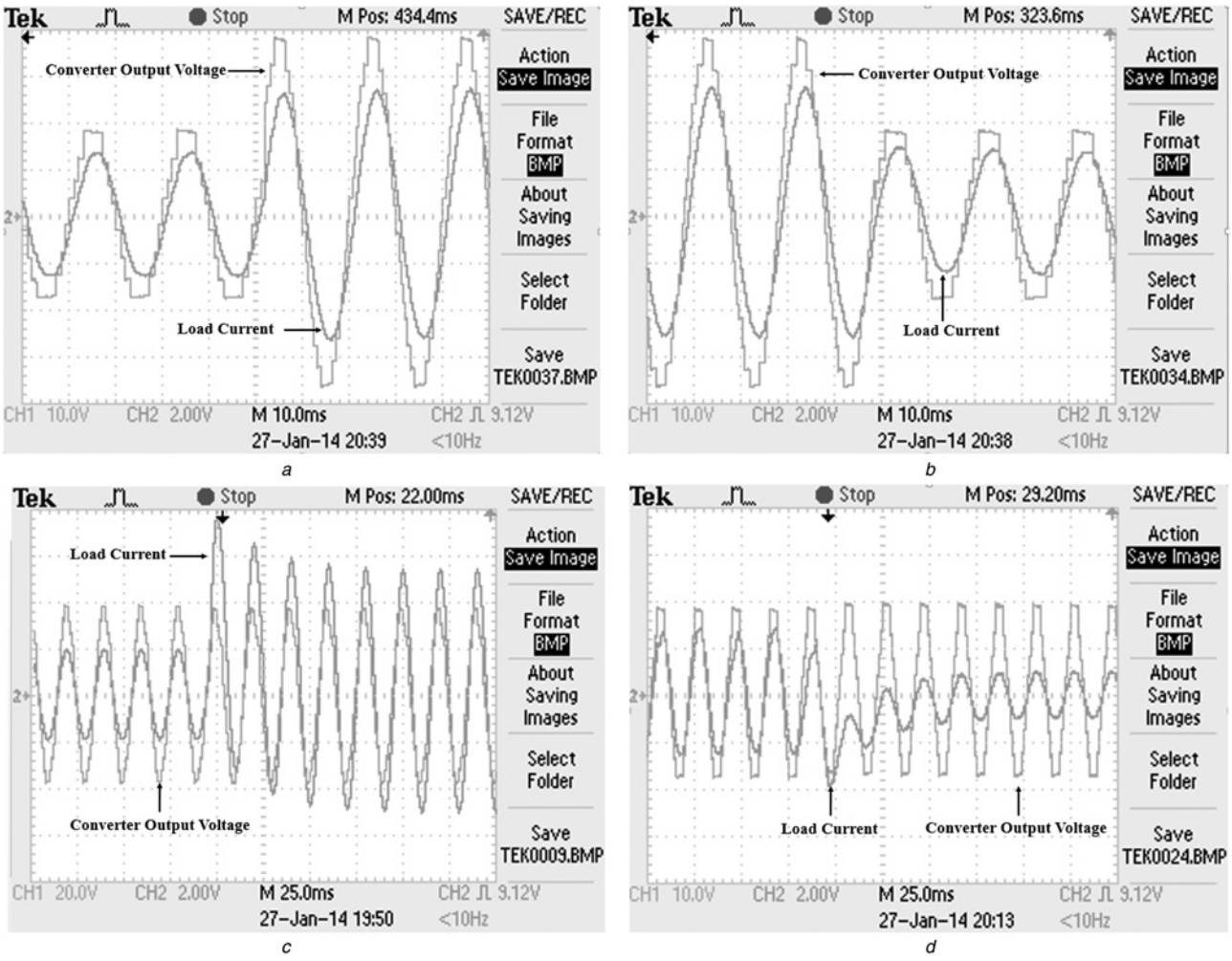


**Fig. 12** *Dynamic behaviour of the 31-level converter for changing the reference voltage from 37 V (peak-to-peak, 8 levels) to 75 V (peak-to-peak, 16 levels)*

*a* 8-level to 16-level
*b* 16-level to 8-level and dynamic behaviour under various load variations
*c* Increasing the load under the 16-level voltage
*d* Decreasing the load under the 8-level voltage
(volt/div = 20 V and 10 V, Amp /div = 2 A)




doi: 10.1049/iet-pel.2013.0872

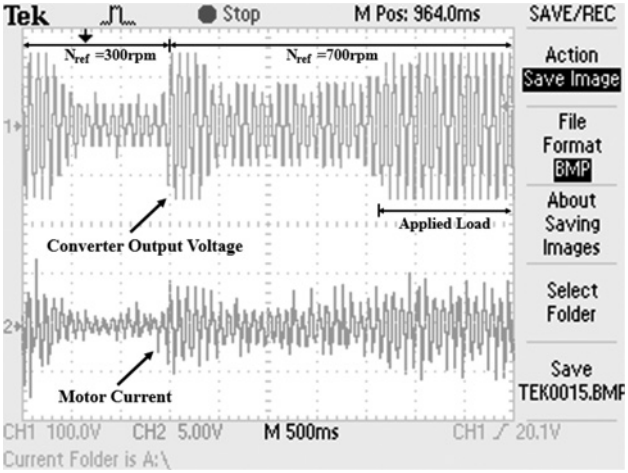


**Fig. 13** *Arranged experiment for the closed-loop control shown in Fig. 7, including the actual output voltage of the converter and the motor current under different working conditions (comparable with those of Fig. 9)*

(volt/div = 100 V, Amp/div = 5 A)

simulations in Fig. 8*a* confirms accurate output voltage build up, having a very close current waveforms along with a small difference in the THD because of practical imperfect parameters.

In addition, the output voltages of the modules as well as the total voltage of the converter are shown in Fig. 11*b*. Also, Figs. 11*c* and *d* demonstrate DC source currents for each module. It is clear from the experimental currents that the middle DC source in each module is identically repeated for every power system half cycle. At the same time, both the bottom and upper DC sources swap their half cycle waveforms in order to assure the energy balance. This helps enforce efficiency in DC sources of each module such that making average currents of modules identical.

Measurements were taken in order to assess the efficiency of the implemented converter. Table 7 provides the average currents of the DC sources within the two modules. These currents along with the voltages of the DC sources lead to active powers of all input DC sources as shown in Table 7 separately; the input power is equal to 317.8 W for the performed experiments, while the switching converter can be loaded up to 5 kVA. The load power can be compared with the total input power to obtain the efficiency of the converter.

*6.2.1 Dynamic load:* Furthermore, assume the reference voltage is changed from 37 V (peak-to-peak, 8 levels) to 75 V (peak-to-peak, 16 levels). Experiments show in Figs. 12*a* and *b* which the load current rises rapidly, describing the fast response in the dynamic behaviour for chasing the voltage variations. Moreover, the load is changed stepwise to demonstrate dynamic behaviour of the 31-level converter as shown in Fig. 12*c* for the 16-level output voltage, and Fig. 12*d* for 8-level. These pictures clearly depict the both fast and proper voltage response of the 31-level converter under a sudden load change.

In addition, the closed-loop control design in Fig. 7 was implemented in order to confirm simulations shown in Fig. 9 in practice. This test describes capability of the suggested class B 31-level converter in supplying the required power of motor. The procedure of starting as well as applying mechanical load is the same as those of simulations in Fig. 9. Experimental results are demonstrated in Fig. 13. Analysis of practical work shows two points; first, the implemented 31-level converter is following the starting as well as dynamics of both load and speed under the closed-loop control in Fig. 7. Second, practical work in Fig. 13 confirms simulations in Fig. 9, illustrating the capability of the 31-level converter in supplying power proportional to the load demand.

*6.2.2 Disturbances on the output voltage:* Assume the implemented inverter is going to be subjected to a typical disturbance on the output voltage under the 31-level operation. Thus, the load power is changed beyond the nominal ratings of the DC-link sources. This causes the source currents to rise significantly, falling down the source voltage levels. Figs. 14*a* and *b* demonstrate both voltages and currents of the inverter for two different operating conditions. When the load current increases, the voltages of the DC sources fall down; consequently, the output voltage of the inverter differs slightly from the desired sinusoidal

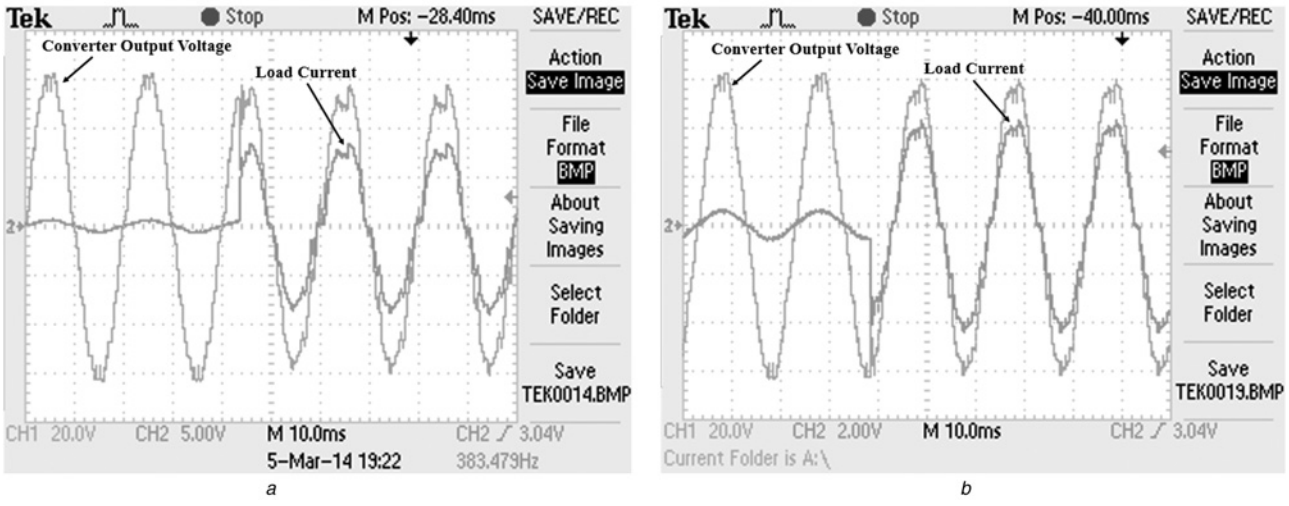


**Fig. 14** *Transition of the load condition from a normal to an overload operation for two different tests*

*a* A severe overload
*b* A light overload
(volt/div = 20 V, Amp/div = 5 and 2 A)

voltage. It can be seen from the pictures that both voltage and current waveforms are distorted under the discussed circumstances when transit from a normal operation to another overloaded operating condition.

## 7 Conclusion

This paper presents a classification scheme based on the reduced structure according to the designs and suggestions appeared on lectures. Two general classes described on the MCRS, including classes A and B with various structures. Among these different structures, structure A2 is considered and its number of switches is rearranged in a way to form a new structure called B2. Classification of the MCRS results in two main conclusions; first, structure A4 is suitable for higher voltage applications, while structure B2 could be applied to low voltage converters along with having a lower number of devices. Structure B2 operates inherently symmetrical in terms of utilisation of the DC sources in each module. Furthermore, a 5 kVA 31-level converter was implemented based on structure B2. This converter is capable of creating 31 levels with a lower number of devices compared with other discussed structures. Experiments as well as simulations are introduced to confirm the validity of the discussions and analysis.

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doi: 10.1049/iet-pel.2013.0872