Published in IET Power Electronics
Received on 2nd December 2012
Revised on 10th July 2013
Accepted on 21st August 2013
doi: 10.1049/iet-pel.2012.0707

ISSN 1755-4535

New concept on sinusoidal modulation for three-phase DC/AC converters: analysis and experiments

Bahman Eskandari[1], *Mohammad Tavakoli Bina*[1], *Masoud Aliakbar Golkar*[2]

[1]*Electrical Faculty, K. N. Toosi University of Technology, Tehran, Iran*
[2]*Department of Electrical Engineering, K. N. Toosi University of Technology, Tehran, Iran*
E-mail: eskandari@ieee.org

Abstract: Various modulation schemes have already been developed for conventional three-phase buck-type converters such as sinusoidal pulse-width modulation and space vector modulation (SVM). However, SVM is not applicable to boost-type converters. This study proposes a new concept on sinusoidal modulation for both buck and boost-type three-phase DC–AC converters. A novel optimised modulation technique is introduced by using basic equations of conventional buck and boost. By solving the optimisation problem, pulse widths will be obtained for a given modulation index. The significant point is that the optimisation problem should not be solved for every modulation index because the answer of the optimisation problem obeys a certain pattern. Also, this method has a positive effect on reducing losses, especially in boost-converters. Analysis and simulations are first introduced for three-phase boost-converters, and then is extended to a buck converter. Furthermore, practical verification takes place on two implemented 1 kVA boost and buck-converters in order to confirm the proposed technique as well as theoretical analysis and simulations. The experiments and simulations both verify the suggested optimised modulation technique.

1 Introduction

Power electronic converters are applied extensively in industry applications as well as other applications in daily life [1, 2]. Their main task is adjustment of the level or conversion to either DC or AC voltage. For example, a boost-inverter combines both the change in the level and DC to AC conversion, providing the operation of a two step solution (DC/DC boost plus DC/AC inversion) all in a single step. The modulator eventually prepares the required signals for the switches of the converter which adjusts the pulse widths. This can take place simply using a PI-controller for a DC/DC converter, while different modulators are applied to the DC/AC converters. A modulation technique affects switching losses, the total harmonic distortion (THD) as well as optimal usage of the DC-link. One main aim of this paper is to establish a new concept on modulation of buck and boost-type three-phase DC/AC converters. This new modulator will make most of the DC source, lowering the DC-link current oscillations, lowering the THD and increasing the efficiency of the converter.

In practice, two steps are taken to achieve the boost-converter tasks; DC–DC boost and DC–AC conversion [3, 4]. For example, these two steps are usually needed in different applications such as photovoltaic generation [5–8]. These two separate converting steps require two independent control loops as well as two modulators. In brief, if these two converters are combined into a boost-converter, then a 'suitable modulator' is capable of lowering the power losses and the THD [9–11]. In [12–15], various topologies are presented that combine the mentioned tasks of the two converters.

The main idea of this paper is to find an efficient modulation technique for the three-phase DC–AC boost and buck-converters. Analysis of the three-phase DC–AC boost-converter in the form of three independent DC–DC boost-converters leads to an efficient optimised modulation technique. The proposed modulation technique for the three-phase boost-converter can also be applied to the buck-type converter (standard six switches two-level converter) mainly because of their structural similarities. Therefore, in the second part of the paper, like that of the three-phase boost-converter, an optimised offset modulation technique is defined for a conventional six-pulse two-level three-phase buck-converter. The performance of the proposed optimised offset modulation technique is compared with those of the common techniques in [16–19] such as carrier-based pulse-width modulation (PWM) and space vector modulation (SVM). Finally, in order to verify the proposed modulation techniques as well as theoretical analysis and simulations, practical verifications are performed on two implemented 1 kVA boost and buck-converter. The outcomes of the suggested technique are accordingly compared with a buck-type DC/AC converter that is identical to a six switch two-level DC/AC

converter driven by the SVM technique. In brief, analysis and experiments show that the proposed modulation technique is mathematically simple to implement, lowers the DC-link current oscillations of the boost-type converter, high efficiency and low THD.

2 Modulating the three-phase DC–AC boost-converter

Among the various topologies of DC–AC converters, boost converter introduces two apparently independent features simultaneously; inverting and increasing the level of input DC voltage. The structure of the three-phase boost-converter is shown in Fig. 1. Looking at the structure, the existence of three independent DC–DC boost-converters is evident. Therefore it is expected that each one of the three DC–DC boost-converters will produce a sinusoidal voltage along with some DC offset. Analysis of the three-phase boost-converter as three separated DC–DC boost type converters is the main theoretical background of this paper. However, producing a pure sinusoidal voltage is hard to achieve because the gain of a real DC–DC boost-converter severely depends on the load current, especially at higher gains. In other words, production of a time-dependent gain (sinusoidal waveform) will include large distortions.

Various modulating techniques were suggested for the three-phase boost-converter in order to generate sinusoidal waveforms; for example, by using adaptive control based on the state space equations [5–8]. Although these complicated control techniques disregard the differential boost structure, this research intentionally concentrates on the differential structure in order to improve the performance in general.

2.1 Suggesting a fixed offset PWM technique for the boost-converter

Assume that the principal goal is to build up three phase-to-phase independent sinusoidal voltages at the load terminal of Fig. 1. The gain of a boost-converter is bigger than or equal to one (when all the controllable switches are off both input and output voltages are identical). Thus, each phase of the boost-converter in Fig. 1 has a DC offset with respect to the negative pole of the battery. Fig. 2 illustrates the amount of this offset, that is, the capacitor voltages V_{aN}, V_{bN} and V_{cN}. Assume that these voltages are modulated

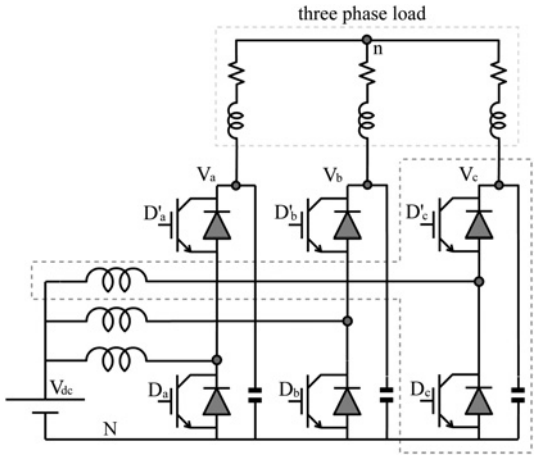


Fig. 1 *Three-phase DC–AC boost-converter*

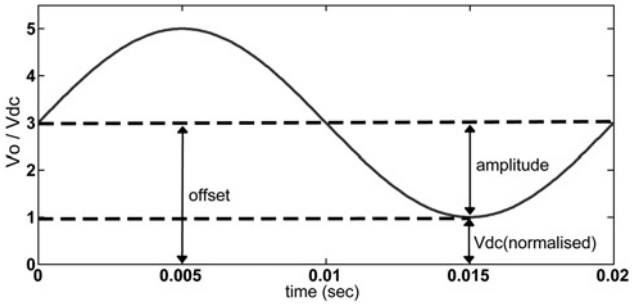


Fig. 2 *Normalised desired output capacitor voltage of one leg in the boost-converter*

with the following duty cycles based on the gain of an ideal DC–DC boost-converter

$$\begin{cases} V_{aN}(t) = \dfrac{V_{\rm dc}}{1-D_a} = A\sin(\omega t) + A + V_{\rm dc} \\ V_{bN}(t) = \dfrac{V_{\rm dc}}{1-D_b} = A\sin(\omega t + 120^\circ) + A + V_{\rm dc} \\ V_{cN}(t) = \dfrac{V_{\rm dc}}{1-D_c} = A\sin(\omega t + 240^\circ) + A + V_{\rm dc} \\ A > V_{\rm dc} \end{cases} \quad (1)$$

where D_a, D_b and D_c are the duty cycles for the three legs, $V_{\rm dc}$ is the DC offset of each boost-converter (the amplitude of the input source) and A is the amplitude of the sinusoidal output voltages. Note that the output voltages of the boost-converter always have identical signs to that of $V_{\rm dc}$; hence, to satisfy this condition, adding the amplitude A to the DC offset (provision of a *fixed offset* $A + V_{\rm dc}$) ensures the mentioned homopolarities.

Subtracting every two boost equations in (1) results in three line voltages V_{ab}, V_{bc} and V_{ca}. It should be pointed out that these line voltages contain no DC component in contrast to the voltages in (1) with respect to N. The point N denotes the negative pole of the DC source, whereas n shows the neutral point of the load. Hence, considering the neutral point n, the desired phase-to-neutral voltages at the load-terminal are $V_{an}(t) = A\sin(\omega t)$, $V_{bn}(t) = A\sin(\omega t - 120^\circ)$ and $V_{cn}(t) = A\sin(\omega t + 120^\circ)$ that are obtained from the relationships and assumptions given in (1). Actually, the value of D for one power period (20 ms) depends on the amplitude of the desired sinusoidal waveform (A) and voltage of the input DC source ($V_{\rm dc}$). To ensure the gain varies above one in (1) for a boost-inverter, $A + V_{\rm dc}$ has to be added to the desired sinusoidal voltage with amplitude A. Therefore the mentioned desired outcomes can be performed in practice by extracting the three-phase duty cycles ($D_a(t)$, $D_b(t)$ and $D_c(t)$) from (1)

$$\begin{cases} D_a(t) = 1 - \dfrac{V_{\rm dc}}{A\sin(\omega t) + A + V_{\rm dc}} \\ D_b(t) = 1 - \dfrac{V_{\rm dc}}{A\sin(\omega t + 120^\circ) + A + V_{\rm dc}} \\ D_c(t) = 1 - \dfrac{V_{\rm dc}}{A\sin(\omega t + 240^\circ) + A + V_{\rm dc}} \end{cases} \quad (2)$$

As an example, let us assume $A = 4 \times 24/\sqrt{3}$ and $V_{\rm dc} = 24$ V; then, the duty cycles for a whole power cycle (20 ms)

doi: 10.1049/iet-pel.2012.0707

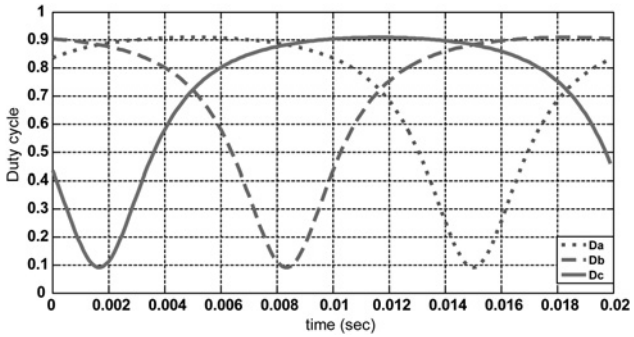


Fig. 3 *Simulated duty cycles by (4)*

are worked out according to (4). Fig. 3 shows these calculated duty cycles.

2.2 Specifications of the implemented boost-converter

A 1 kVA boost-converter was implemented according to Fig. 1. Table 1 provides the detailed specifications of the test setup. This is used as a practical prototype for evaluating the performance of the suggested modulation technique. The power circuit includes two series 12 V, 55 Ah batteries as the input DC voltage V_{dc}, three 200 μH inductors (10 A), three 250 μF capacitors (100 V) and six IGBTs (BUP314D). Drivers of the switches are fed through four isolated DC supplies, where the coupler TLP250 interfaces with the microprocessor and the power circuit. A three-phase laboratory L-C set as the output filter and a 2 kW, 380 V induction motor were used as the load. The microprocessor is the EZDSP TMS320F28335 that regulates pulse widths for the six switches using code composer studio (CCSTUDIO). Fig. 4 shows the implemented three-phase boost-converter described above.

2.3 Description and analysis of the experimental results

Typical calculated duty cycles shown in Fig. 3 were programmed with CCSTUDIO on EZDSPF28335 to drive the six switches of the boost-converter. Three phase-to-neutral voltages (V_{an}, V_{bn} and V_{cn}) and three phase-to-negative poles of the DC source (V_{aN}, V_{bN} and V_{cN}) were recorded through a serial port as shown in Fig. 5. Studying Fig. 5*a* shows clearly the amount of added DC offset to all three phases. Also, the difference between the two outputs of the individual DC–DC boost-converters (V_{cN}–V_{bN}) is shown in Fig. 5*b*, where the presence of the L-C filters removes the high frequency ripples of the load voltages. The significant point is that the experiments agree well with the simulations.

Table 1 Specifications of the laboratory three-phase boost-type converter

No.	Title	Specifications	Quantity
1	IGBT	BUP314, 35 A and 1200 V	6
2	capacitor	250 μF and 100 V	6
3	inductor	200 μH and 10 A	3
4	battery	12 V and 55 Ah	2
5	driver	TLP 250, ±30 V and 1 A	6
6	three-phase laboratory L-C set	2 mH and 15 A	1
7	switching frequency	—	10 kHz
8	fundamental frequency	—	50 Hz
9	input voltage	—	24 V DC
10	output line voltage (rms)	—	120 V
11	microprocessor	EZDSP TMS320F28335	1

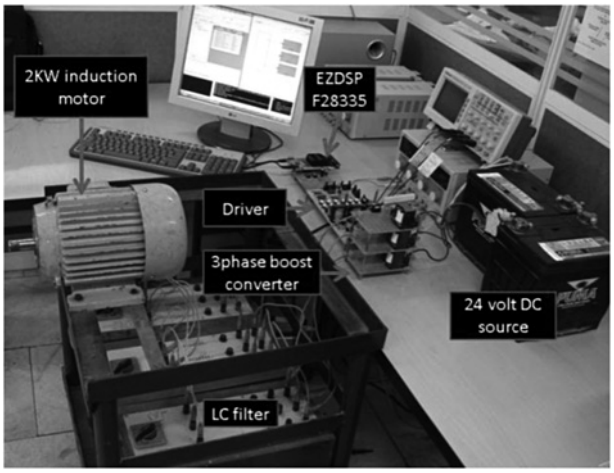
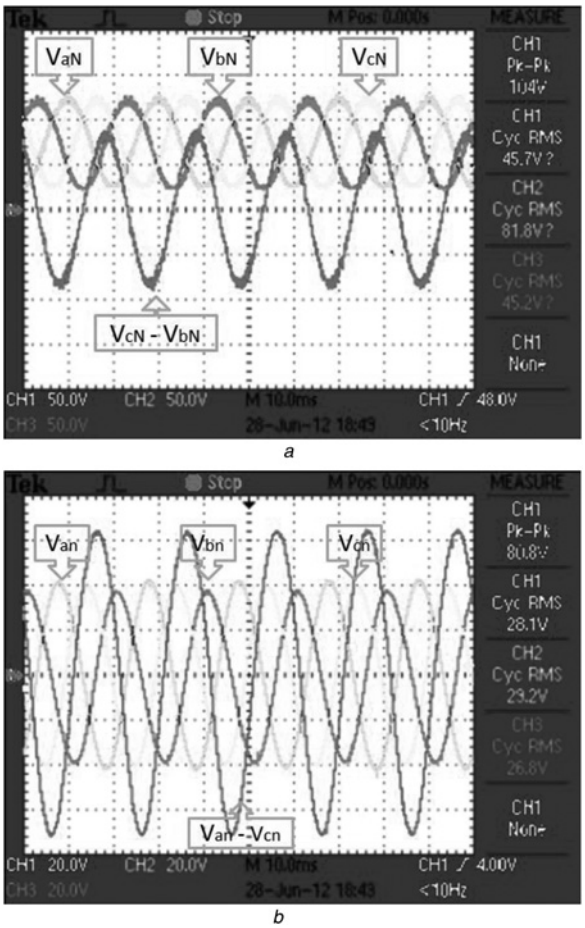


Fig. 4 *Implemented three-phase 1 kVA boost-converter for studying the suggested modulation techniques*



a

b

Fig. 5 *Experimental results*

a Three phase-to-negative voltages
b Three phase-to-neutral voltages

2.4 Offset optimisation

Practical work verifies that the proposed fixed offset modulator is capable of producing three-phase sinusoidal voltages with bigger amplitude compared with the source voltage (V_{dc}). Interestingly, reduction of this fixed offset will pave the way for efficient generation of sinusoidal output voltages because of lower duty cycles. Furthermore, investigating the possibility of 'varying the DC offset' instead of working with a 'fixed offset' comes to mind. Hence, let the total offset be variable, named as $X(t)$. Then, relationships (1) can be rearranged as follows

$$\begin{cases} V_{aN}(t) = \dfrac{V_{dc}}{1-D_a} = A\sin(\omega t) + X(t) \\ V_{bN}(t) = \dfrac{V_{dc}}{1-D_b} = A\sin(\omega t + 120^\circ) + X(t) \\ V_{cN}(t) = \dfrac{V_{dc}}{1-D_c} = A\sin(\omega t + 240^\circ) + X(t) \\ V_{aN}(t) + V_{bN}(t) + V_{cN}(t) = 3X(t) \end{cases} \quad (3)$$

Thus, the aim is to minimise the variable DC offset $X(t)$ or $V_{aN}+V_{bN}+V_{cN}$. In fact, an optimisation problem is defined to achieve a 'time-dependent minimised offset' as follows

$$\text{minimise: } V_{aN}(t) + V_{bN}(t) + V_{cN}(t)$$

$$\text{Subjected to: } \begin{cases} V_{aN}(t) - V_{bN}(t) = \sqrt{3}A\sin(\omega t - 30) \\ V_{bN}(t) - V_{cN}(t) = \sqrt{3}A\sin(\omega t + 90^\circ) \\ V_{aN}(t) \geq 1,\ V_{bN}(t) \geq 1,\ V_{cN}(t) \geq 1 \\ A \geq 1 \end{cases} \quad (4)$$

The normalised value of $\sqrt{3}A$ is equal to 4 for the given example of Fig. 3. Solving the above optimisation problem needs to be repeated for several points during one period of power frequency f_p. If f_s is the switching frequency, then the number of points is equal to f_s/f_p. Throughout this paper, f_p and f_s are 50 Hz and 10 kHz, respectively; therefore, the number of samples will be 200 points. The optimisation problem (4) was repeated to solve all the 200 points as shown in Fig. 6*a*. The new three-phase duty cycles will be concluded by replacing the obtained outcomes of the optimisation problem in (3) with $X(t)$.

The results of the optimisation problem for each phase demonstrate interesting regularly repeated shapes. It can be seen from Fig. 6*a* that the variable DC offset is divided into four certain patterns; combining the DC offset numbered as 1 with that of 4 results in a unified mirror of part 2. Part 3 introduces no DC offset. Fig. 6*b* demonstrates three duty cycles under the variable DC offset. To verify the performance of the proposed optimisation method, these optimised calculated duty cycles are applied to the implemented boost-converter. The experimental results are shown in Figs. 6*c* and *d*, confirming the proposed analysis and the simulations.

2.5 Analytical discussions

An analytical comparison can be studied based on experiments on both the fixed and the optimised offset techniques to find out their performances in practice. To establish a valid comparison, identical amplitudes for line voltages are considered at the load terminals for both techniques (4 × 24 V). The boost-inverter was uploaded by the two modulating techniques, and their corresponding outcomes were recorded for further discussions.

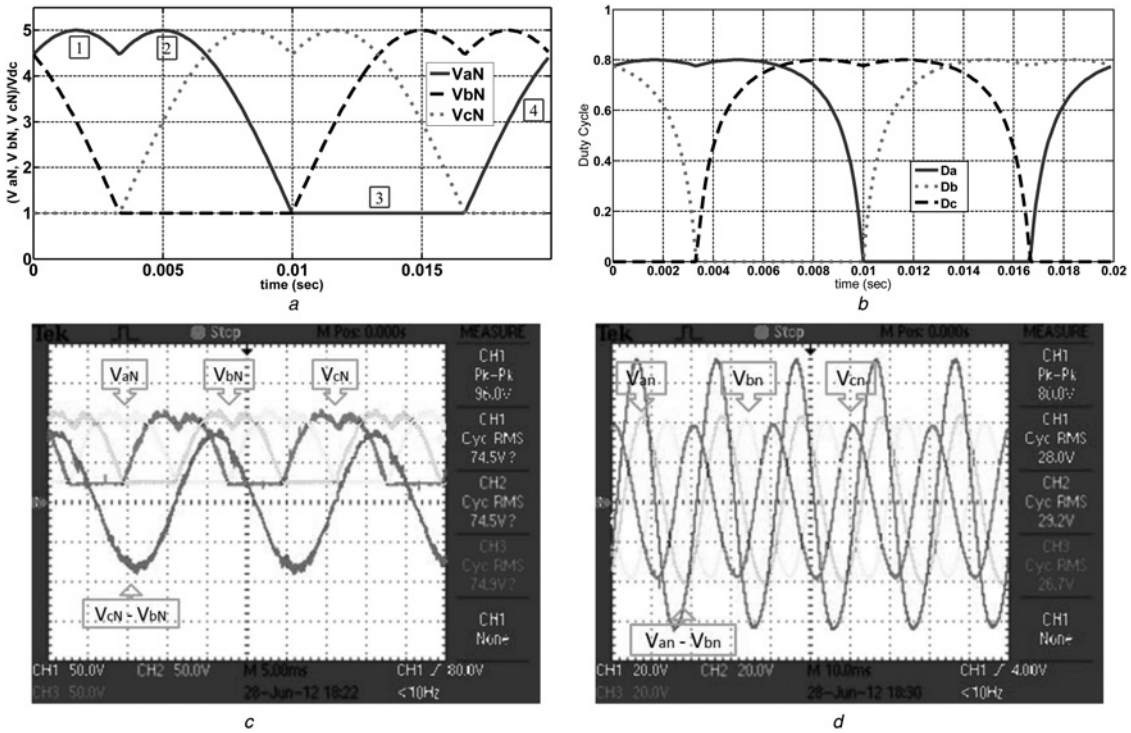


Fig. 6 *Optimisation results*

a Three phase-to-negative voltages
b Produced duty cycles by *5* Experimental results (minimised offset for boost-converter)
c Three phase-to-negative voltages
d Three phase-to-neutral voltages

doi: 10.1049/iet-pel.2012.0707

Fig. 7*a* shows the DC offset $(V_{aN}+V_{bN}+V_{cN})/3$ obtained by the two suggested modulation techniques. Although, the produced offset by the optimised technique is smaller than the fixed offset throughout a power period (20 ms), removing part of the needed active power because of the harmonics from the source. It should be noted that a lower total DC offset in (2) would result in lower turn on times of the switches. Furthermore, generated fundamental voltages are introduced in Fig. 7*b*, where their THD were also calculated by obtaining the spectra of the output voltages as demonstrated in Fig. 7*c*. These pictures state that the optimised offset provides slightly bigger fundamental compared with the fixed offset. Also, the THD for the fixed and the optimised techniques are 6% and 4%, respectively. Moreover, both the input and the output currents for the two techniques can be compared in Fig. 7*d*. It is clear that the DC source current is considerably lower for the optimised offset under the same loading conditions in comparison with the fixed offset. At the same time, the phase of the output current is much closer to the fundamental output voltage for the optimised offset. In addition, Figs. 8*a* and *b* present the optimised offset (V_{aN}), both simulations and experiments strongly confirm the theoretical discussions and analysis.

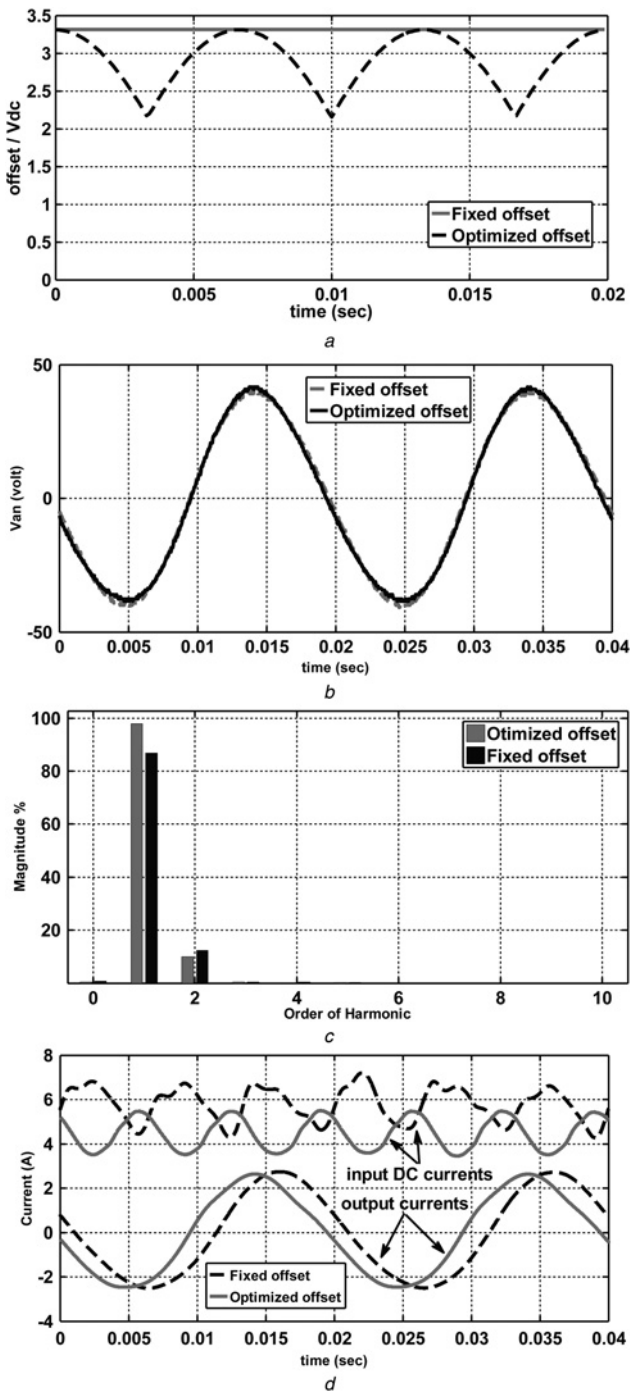


Fig. 7 *Comparison between*

a Amount of fixed and optimised offset
b Output voltages (V_{an})
c Spectrum of output voltages
d Input and output currents of both techniques

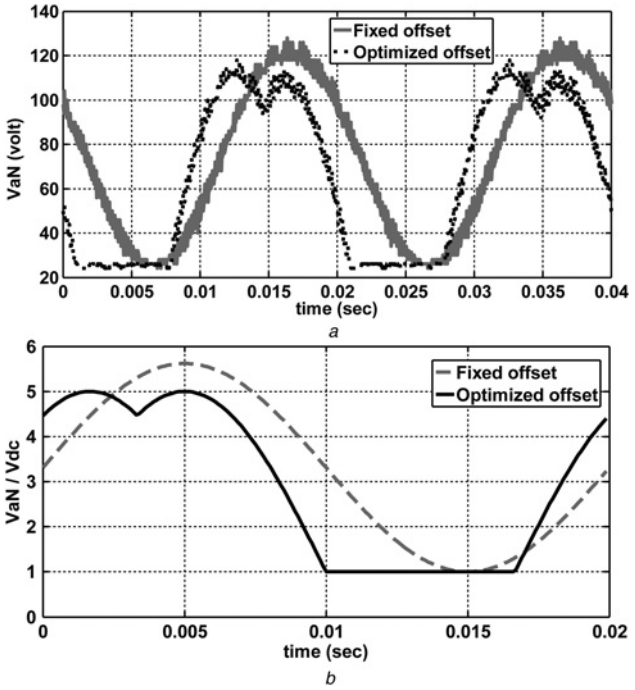


Fig. 8 *Output voltages (V_{aN}) of both techniques*

a Experiments
b Simulations

3 Modulating the three-phase buck-converter

Consider the three-phase differential buck-converter shown in Fig. 9*a*. There are two conventional modulation techniques for utilising the three-phase buck-converters; carrier based methods (CBM) and SVM. Although the CBM are simple to implement, they limit the modulation index to 86%. However, the modulation index of the SVM could be even greater than one in some parts of the hexagonal frame. Implementation of the SVM needs fast digital processors because of heavy computational load. In this section, relationship (1) is rearranged for the three-phase buck-converter, where both fixed and optimised offsets will be theoretically discussed and implemented as the modulation techniques.

3.1 Fixed offset (or the CBM) modulation technique

Like the three-phase boost-converters, the buck-type three-phase converters also consist of three separate

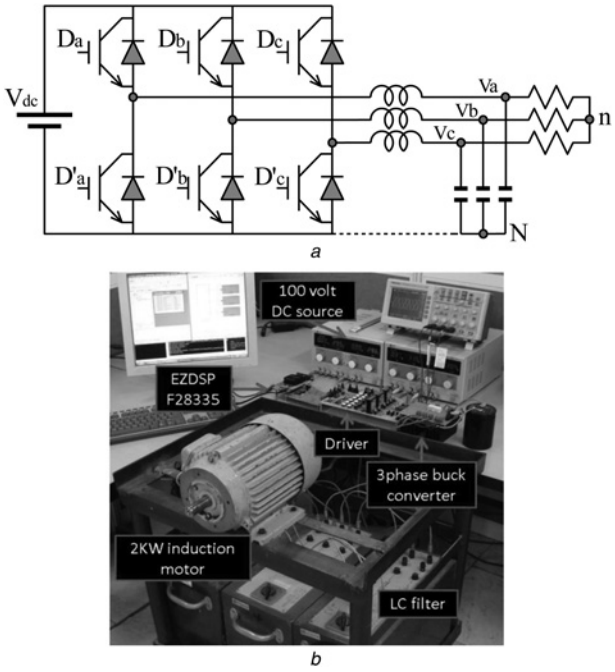


Fig. 9 *Three-phase differential buck-converter*

a Circuit of the three-phase buck-converter
b Implemented three-phase buck-converter

differential DC–DC buck-converters. Since the line voltages at the load terminal are obtained by differentiating two phase voltages and no DC stress is imposed to the load; because the DC offset is identical for all the phases. One simple solution for the modulation would be generation of three independent CBM sinusoidal PWM with 120° phase shift. Furthermore, the SVM is an efficient technique for direct calculation of duty cycles. Meanwhile, it is also possible to utilise the offset technique by adding a fixed offset equal to the amplitude of the desired sin-wave for the three-phase buck-converter as follows

$$\begin{cases} \dfrac{V_{aN}(t)}{V_{\mathrm{dc}}} = D_a(t) = A\sin(\omega t) + A \\ \dfrac{V_{bN}(t)}{V_{\mathrm{dc}}} = D_b(t) = A\sin(\omega t + 120^\circ) + A \\ \dfrac{V_{cN}(t)}{V_{\mathrm{dc}}} = D_c(t) = A\sin(\omega t + 240^\circ) + A \\ 0 \le D(t) \le 1 \Rightarrow A \le 0.5 \end{cases} \quad (5)$$

Based on the duty cycle limits, the fixed offset A has to be bounded to 0.5. Hence, the maximum amplitude of the line voltage (normalised by V_{dc}) is limited to $0.5 \times \sqrt{3} \simeq 0.86$. This clearly indicates a 14% reduction in the modulation index as a disadvantage for (7). Thus, the fixed offset modulation performs in this aspect similar to the conventional sinusoidal PWM technique.

Fig. 10*b* shows a 1 kVA three-phase differential buck-converter that was implemented based on Fig. 9*a*; Table 2 shows the detailed implementation specifications. This is used as a practical prototype for evaluating the performance of conventional modulation techniques such as the CBM (or fixed offset) and the SVM in comparison with the proposed optimised offset modulation. Starting with the CBM and considering $A = 0.5$, the calculated duty cycles for one power cycle are shown in Fig. 10*a*. The simulations

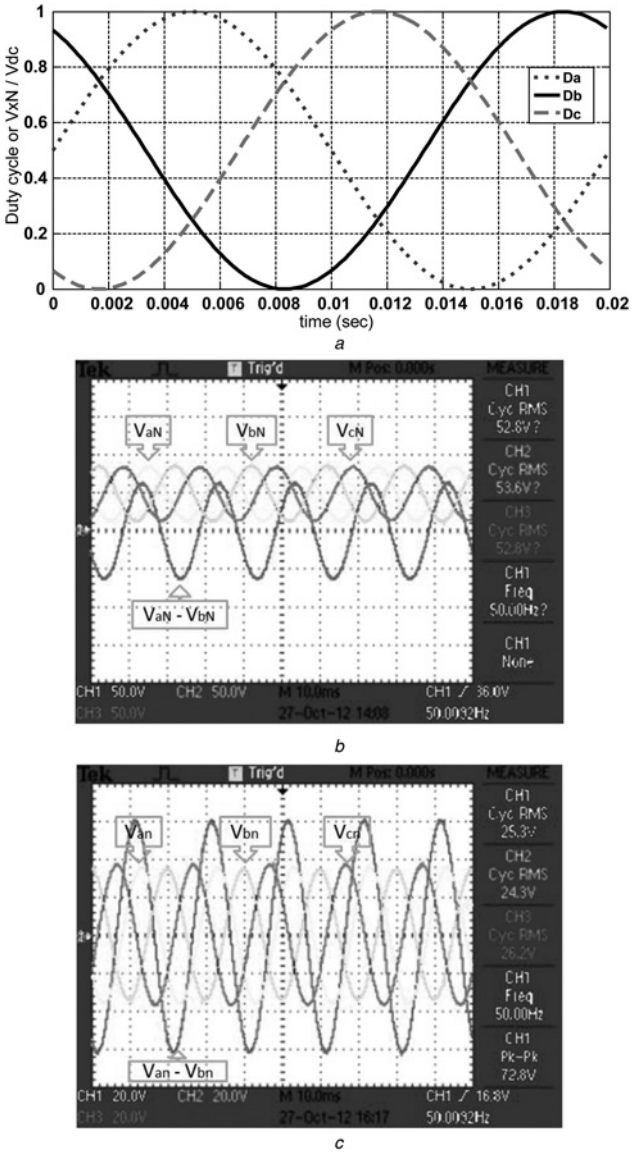


Fig. 10 *Experimental results for the three-phase buck-converter because of the CBM (or fixed offset technique)*

a Calculated three-phase duty cycles by (7) for $A = 0.5$
b Three phase-to-negative voltages
c Three phase-to-neutral voltages

in Fig. 10*a* can be compared with the experiment shown in Figs. 10*b* and *c*. It can be seen that the offset in Fig. 10*b* is limited to 0.5, whereas Fig. 10*c* presents the load voltages with their related effective values.

3.2 Application of the SVM

Here, the SVM has also been implemented in order to have a useful comparison with other experiments. The output voltages because of the SVM (modulation index = 1) are shown in Figs. 11*a* and *b*. Comparing the RMS values in Fig. 10*c* because of the CBM with those of Fig. 11*b* (the SVM) indicates that the load voltages are increased.

3.3 Applying offset optimisation

It is possible to increase the modulation index by using the proposed offset optimisation technique. First, the fixed

doi: 10.1049/iet-pel.2012.0707

Table 2 Specifications of the laboratory three-phase buck-type converter

No.	Title	Specifications	Quantity
1	IGBT	BUP314, 35 A and 1200 V	6
2	capacitor	250 μF and 100 V	3
4	power supply	60 V and 5 A	2
5	driver	TLP 250, ±30 V and 1 A	6
6	three-phase laboratory L-C set	2 mH and 15 A	1
7	switching frequency	10 kHz	
8	fundamental frequency	50 Hz	
9	input voltage	100 V DC	
10	output line voltage (rms)	70 V	
11	microprocessor	EZDSP TMS320F28335	1

offset A in (5) is replaced with an unknown time dependent $X(t)$ given as follows

$$\begin{cases} \dfrac{V_{aN}(t)}{V_{\rm dc}} = D_a(t) = A\sin(\omega t) + X(t) \\ \dfrac{V_{bN}(t)}{V_{\rm dc}} = D_b(t) = A\sin(\omega t + 120^\circ) + X(t) \\ \dfrac{V_{cN}(t)}{V_{\rm dc}} = D_c(t) = A\sin(\omega t + 240^\circ) + X(t) \\ \dfrac{V_{aN}(t) + V_{bN}(t) + V_{cN}(t)}{3 \times V_{\rm dc}} = X(t) \\ 0 \le D(t) \le 1 \end{cases} \quad (6)$$

Summation of the three first relationships shows that $X(t)$ is proportional to the sum of the three-phase voltages. Therefore the objective function can be set out as minimising the sum of the three-phase voltages with respect to the DC negative pole N

$$\text{minimise: } V_{aN}(t) + V_{bN}(t) + V_{cN}(t)$$

$$\text{Subjected to: } \begin{cases} V_{aN}(t) - V_{bN}(t) = \sqrt{3}A\sin(\omega t - 30^\circ) \\ V_{bN}(t) - V_{cN}(t) = \sqrt{3}A\sin(\omega t + 90^\circ) \\ V_{aN}(t),\ V_{bN}(t),\ V_{cN}(t) \ge 0 \\ \sqrt{3}A \le 1 \end{cases} \quad (7)$$

Assume that $\sqrt{3}A$ is equal to one for the maximum line voltage amplitude. Then, solving (7) results in illustration of the optimised duty cycles in Fig. 12. The outcome is very significant because no switching operation is required in 33% of the power cycle for each leg of the buck-type converter. In addition, the modulation index can be raised to one. Also, like the boost-converter, the outcomes of the optimisation problem (7) follow a certain pattern. The calculated duty cycles in Fig. 12 have been implemented on the buck-type converter of Fig. 9*b*, and the recorded results are shown in Figs. 13 and 14. It is clear that the obtained results are very similar to those of the SVM.

3.4 Discussion on the three modulation techniques

Three implemented modulation techniques for the conventional two-level three-phase buck-type converter can be compared in terms of three major aspects. First, the

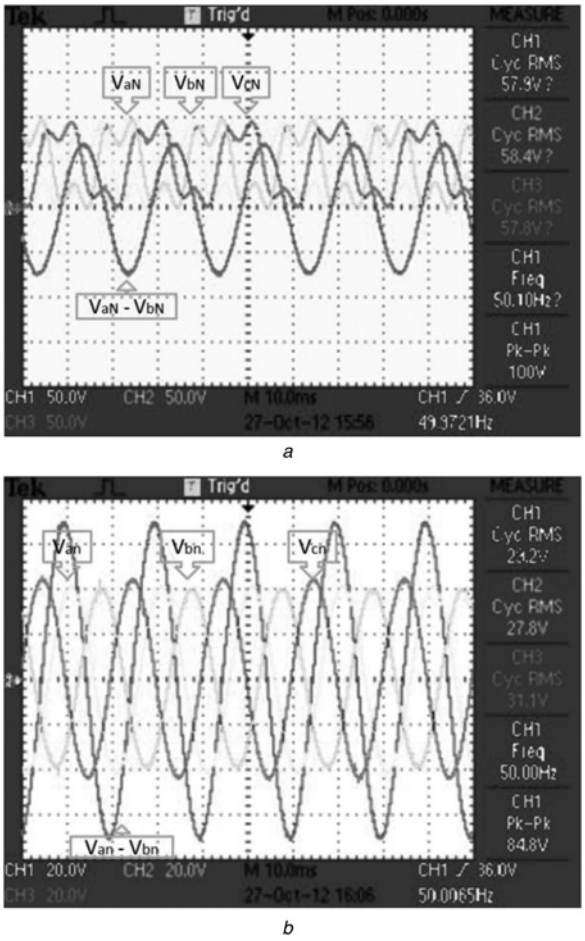


Fig. 11 *Experimental results for the three-phase buck-converter because of the SVM technique*

a Three phase-to-negative voltages
b Three phase-to-neutral voltages

modulation index for the optimied offset proposal is equal to one like that of the SVM. However, the modulation index for the fixed offset technique is smaller than 0.86 as shown in Fig. 15*b*. Second, the switching number as well as the switching losses in the optimied offset modulation are approximately 33% smaller than the other two techniques. Third, the output voltages because of the offset optimisation are very similar to those of the SVM (see Figs. 14*b* and 15*b*), while the computational load of the optimised technique is much less than the SVM. The generated offsets by the three mentioned techniques are compared in Fig. 15*a*. Interestingly, the generated offset by

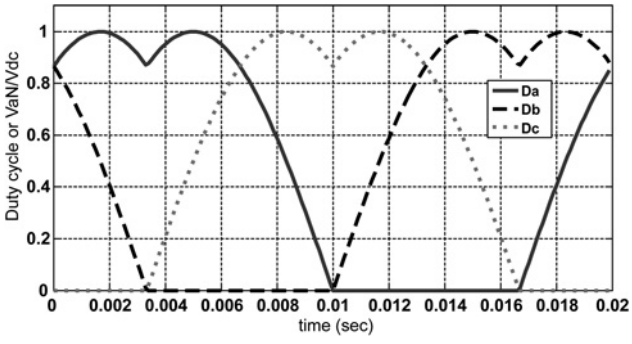


Fig. 12 *Simulations of (9) when* $\sqrt{3}A = 1$

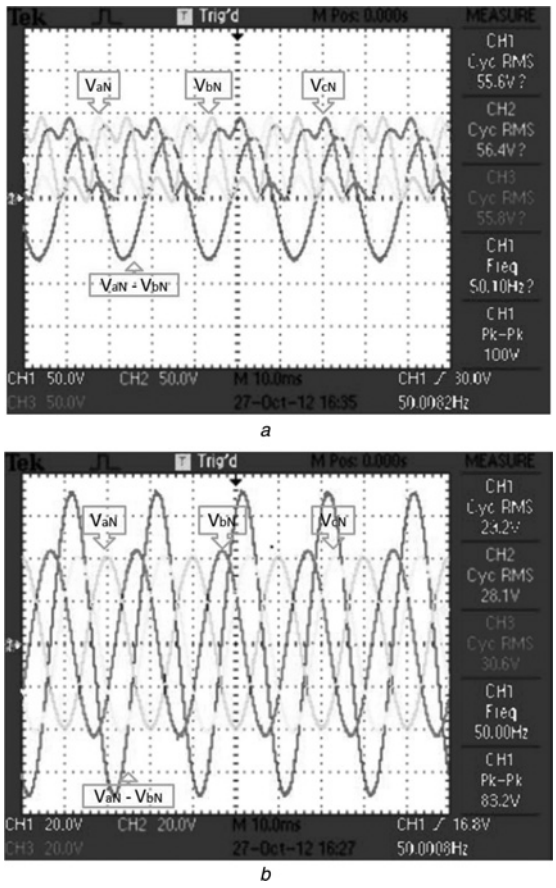


Fig. 13 *Experimental results for the three-phase buck-converter because of the optimised offset technique*

a Three phase-to-negative voltages
b Three phase-to-neutral voltages

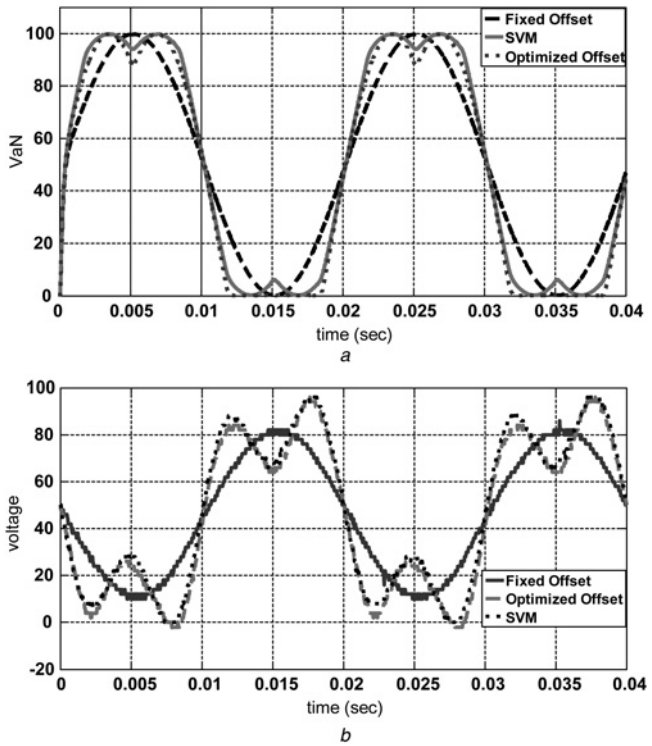


Fig. 14 *Comparison between V_{aN} obtained from the implementation of the three different modulation techniques*

a Simulations
b Experiments

the SVM introduces a larger peak than the generated offset through the optimisation technique. Meanwhile, Fig. 15*c* provides a stronger comparison between the fixed offset (or the CBM), the SVM and the optimised offset in terms of their generated low order harmonics up to the 11th. It is clear from Figs. 15*a–d* that both the optimised offset and

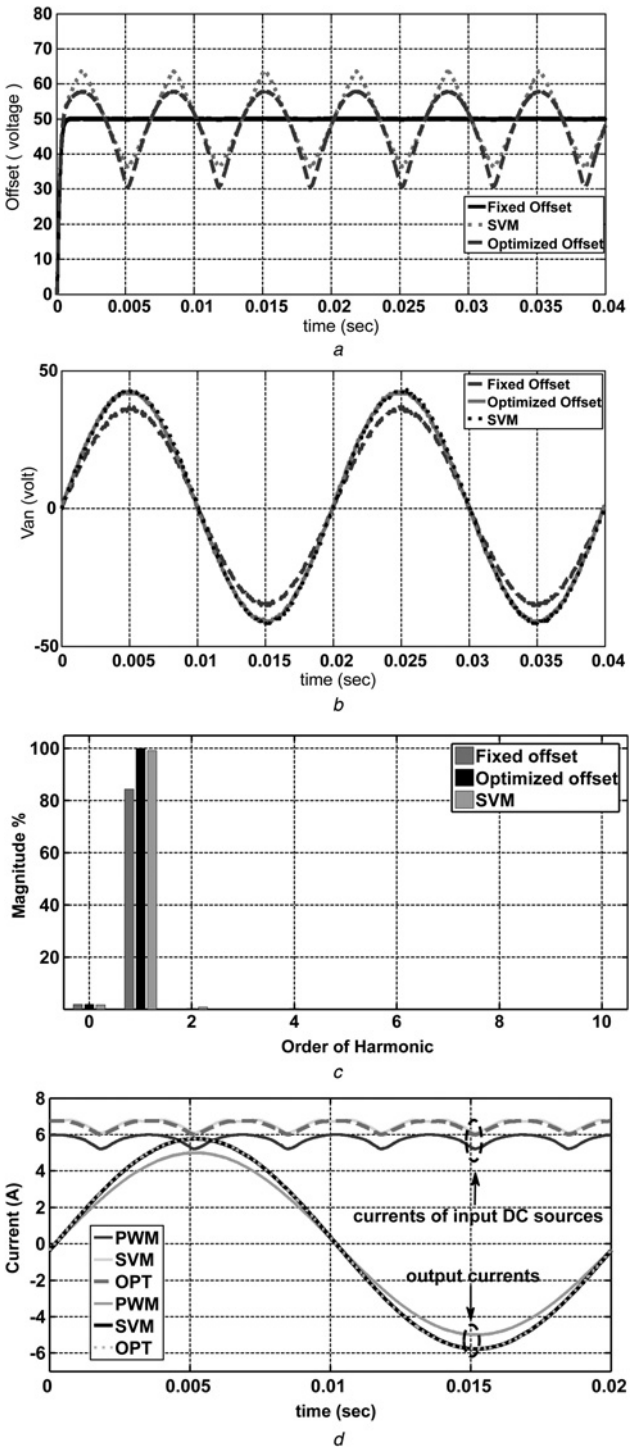


Fig. 15 *Modulation techniques for conventional two-level three-phase buck type converter*

a Simulated DC offset because of the three modulation techniques
b Practical V_{an} because of the three modulation techniques
c Spectrum of output voltages because of the three modulation techniques
d Comparison between the input and the output currents because of the three modulation techniques

doi: 10.1049/iet-pel.2012.0707

the SVM perform very similarly, while the fixed offset generates a limited fundamental up to 86%.

4 Conclusion

This paper analyses the structures of the three-phase differential boost-type and buck-type converters based on three separate DC–DC boost-converters. It is shown that the DC offset plays an important role in the modulation techniques. An efficient modulation technique, the optimised offset modulation, is proposed that is applicable to the three-phase converters. Major contributions of the proposed modulating strategy include lower calculations and lower DC-link current oscillations in boost-type converters compared with the other strategies. Two experimental test sets were designed to evaluate the proposed modulation techniques for both the boost and the buck-converters. The experimental results of the boost-converter indicate considerable effects on the improved modulation as well as current reduction of the DC source. Also, the results of the implementation of the optimised offset modulation on the buck-converter are very similar to that of the SVM. The proposed optimisation technique has two major advantages compared with the SVM; 33% lower switching losses and simplicity in implementation.

5 References

1 Shen, J.M., Jou, H.L.: 'Transformer-less three-port grid-connected power converter for distribution power generation system with dual renewable energy sources', *IET Power Electron.*, 2012, **5**, (4), pp. 501–509

2 Sun, K., Zhang, L., Xing, Y., Guerrero, J.M.: 'A distributed control strategy based on DC bus signaling for modular photovoltaic generation systems with battery energy storage', *IEEE Trans. Power Electron.*, 2011, **26**, (4), pp. 3032–3045

3 Liang, Z., Guo, R., Li, J., Huang, A.Q.: 'A high-efficiency PV module-integrated DC/DC converter for PV energy harvest in FREEDM systems', *IEEE Trans. Power Electron.*, 2011, **26**, (3), pp. 897–909

4 Cecati, C., Dell'Aquila, A., Liserre, M.: 'A novel three-phase single-stage distributed power inverter', *IEEE Trans. Power Electron.*, 2004, **19**, (5), pp. 1226–1233

5 Yufei, Z., Wenxin, H.: 'Single-stage boost inverter with coupled inductor', *IEEE Trans. Power Electron.*, 2012, **27**, (4), pp. 1885–1893

6 Gautam, D.S., Bhat, A.K.S.: 'A Comparison of soft-switched DC-to-DC converters for electrolyzer application', *IEEE Trans. Power Electron.*, 2013, **28**, (1), pp. 54–63

7 Valderrama-Blavi, H., Bosque, J.M., Guinjoan, F., Martínez-Salamero, L.M.: 'Power adaptor device for domestic DC micro gridsbased on commercial MPPT inverters', *IEEE Trans. Ind. Electron.*, 2013, **60**, (3), pp. 1191–1203

8 Gu, B., Dominic, J., Lai, J., Liu, Z.Z.C.: 'High boost ratio hybrid transformer DC–DC converter for photovoltaic module applications', *IEEE Trans. Power Electron.*, 2013, **28**, (4), pp. 2048–2058

9 Jang, M., Ciobotaru, M., Agelidis, V.G.: 'A single-phase grid-connected fuel cell system based on a boost-inverter', *IEEE Trans. Power Electron.*, 2013, **28**, (1), pp. 279–288

10 Mirafzal, B., Saghaleini, M., Kaviani, A.K.: 'An SVPWM-based switching pattern for stand-alone and grid-connected three-phase single-stage boost inverters', *IEEE Trans. Power Electron.*, 2011, **26**, (4), pp. 1102–1111

11 Chang, Y.: 'Design and analysis of multistage multiphase switched-capacitor boost DC–AC inverter', *IEEE Trans. Circuit Syst.*, 2011, **58**, (1), pp. 205–218

12 Zhu, M., Yu, K., Luo, F.L.: 'Switched inductor Z-source inverter', *IEEE Trans. Power Electron.*, 2010, **25**, (8), pp. 2150–2158

13 Rezvanyvardom, M., Adib, E., Farzanehfard, H.: 'New interleaved zero-current switching pulse-width modulation boost converter with one auxiliary switch', *IET Power Electron.*, 2011, **4**, (9), pp. 979–983

14 Chen, Y., Smedley, K.: 'Three-phase boost-type grid-connected inverter', *IEEE Trans. Power Electron.*, 2008, **23**, (5), pp. 2301–2309

15 Hausmann, R., Barbi, I.: 'Three-phase DC–AC converter using four-state switching cell', *IEEE Trans. Power Electron.*, 2011, **26**, (7), pp. 1857–1867

16 Zhang, D., Wang, F., El-Barbari, S., Sabate, J.A., Boroyevich, D.: 'Improved asymmetric space vector modulation for voltage source converters with low carrier ratio', *IEEE Trans. Power Electron.*, 2012, **27**, (3), pp. 1130–1140

17 Govindaraju, C., Baskaran, K.: 'Efficient sequential switching hybrid-modulation techniques for cascaded multilevel inverters', *IEEE Trans. Power Electron.*, 2011, **26**, (3), pp. 1639–1648

18 Dupczak, B.S., Perin, A.J., Heldwein, M.L.: 'Space vector modulation strategy applied to interphase transformers-based five-level current source inverters', *IEEE Trans. Power Electron.*, 2012, **27**, (6), pp. 2740–2751

19 Lai, Y.S., Lin, Y.K., Chen, C.W.: 'New hybrid pulsewidth modulation technique to reduce current distortion and extend current reconstruction range for a three-phase inverter using only DC-link sensor', *IEEE Trans. Power Electron.*, 2013, **28**, (3), pp. 1331–1337